

# PXI Express™

## NI PXIe-1062Q User Manual

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# About This Manual

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The *NI PXIe-1062Q User Manual* describes the features of the NI PXIe-1062Q chassis and contains information about configuring the chassis, installing the modules, and operating the chassis.

## Conventions

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The following conventions are used in this manual:

»

The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **Options»Settings»General** directs you to pull down the **Options** menu, select the **Settings** item, and select **General** from the last dialog box.



This icon denotes a note, which alerts you to important information.



This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on the product, refer to the *Read Me First: Safety and Electromagnetic Compatibility* document, shipped with the product, for precautions to take.

**bold**

Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names.

*italic*

Italic text denotes variables, emphasis, a cross-reference, or an introduction to a key concept. Italic text also denotes text that is a placeholder for a word or value that you must supply.

monospace

Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames, and extensions.

## Related Documentation

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The following documents contain information that you might find helpful as you read this manual:

- IEEE 1101.1-1991, *IEEE Standard for Mechanical Core Specifications for Microcomputers Using IEC 603-2 Connectors*
- IEEE 1101.10, *IEEE Standard for Additional Mechanical Specifications for Microcomputers Using IEEE 1101.1 Equipment Practice*
- *PICMG EXP.0 R1.0 CompactPCI Express Specification*, PCI Industrial Computers Manufacturers Group
- *PCI Express Base Specification*, Revision 1.1, PCI Special Interest Group
- *PXI-5 PXI Express Hardware Specification*, Revision 2.0, PXI Systems Alliance



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# Getting Started

This chapter describes the key features of the NI PXIe-1062Q chassis and lists the kit contents and optional equipment you can order from National Instruments.

## Unpacking

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Carefully inspect the shipping container and the chassis for damage. Check for visible damage to the metal work. Check to make sure all handles, hardware, and switches are undamaged. Inspect the inner chassis for any possible damage, debris, or detached components. If damage appears to have been caused during shipment, file a claim with the carrier. Retain the packing material for possible inspection and/or reshipment.

## What You Need to Get Started

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The NI PXIe-1062Q chassis kit contains the following items:

- ☐ NI PXIe-1062Q chassis
- ☐ Filler panels
- ☐ AC power cable—refer to Table 1-1 for AC power cables
- ☐ *NI PXIe-1062Q User Manual*
- ☐ Software media with *PXI Platform Services 2.0* or higher
- ☐ *Read Me First: Safety and Electromagnetic Compatibility*
- ☐ Chassis number labels

**Table 1-1.** AC Power Cables

| Power Cable          | Reference Standards           |
|----------------------|-------------------------------|
| Standard 120 V (USA) | ANSI C73.11/NEMA 5-15-P/IEC83 |
| Switzerland 220 V    | SEV                           |
| Australia 240 V      | AS C112                       |
| Universal Euro 230 V | CEE (7), II, IV, VII IEC83    |
| North America 120 V  | ANSI C73.20/NEMA 5-15-P/IEC83 |
| United Kingdom 230 V | BS 1363/IEC83                 |

If you are missing any of the items listed in Table 1-1, or if you have the incorrect AC power cable, contact National Instruments.

## Key Features

The NI PXIe-1062Q chassis combines a high-performance 8-slot PXI Express backplane with a high-output power supply and a structural design that has been optimized for maximum usability in a wide range of applications. The chassis' modular design ensures a high level of maintainability, resulting in a very low mean time to repair (MTTR). The NI PXIe-1062Q chassis fully complies with the *PXI-5 PXI Express Hardware Specification*, offering advanced timing and synchronization features.

The key features of the NI PXIe-1062Q chassis include the following:

### High Performance for Instrumentation Requirements

- Up to 1 GB/s (single direction) per PXI Express slot dedicated bandwidth (x4 PCIe)
- 353.9 W available power for 0 to 55 °C
- 30 W per slot cooling meets increased PXI Express cooling requirements
- Low-jitter internal 10 MHz reference clock for PXI slots with  $\pm 25$  ppm stability
- Low-jitter internal 100 MHz reference clock for PXI Express slots with  $\pm 25$  ppm stability
- Quiet operation for 0 to 30 °C at 43.6 dBA

- Variable speed fan controller optimizes cooling and acoustic emissions
- Remote power-inhibit control
- Complies with PXI and CompactPCI Specifications

## **High Reliability**

- 0 to 55 °C extended temperature range
- Power supply, temperature, and fan monitoring
- HALT tested for increased reliability
- Field replaceable power supply shuttle

## **Multi-Chassis Support**

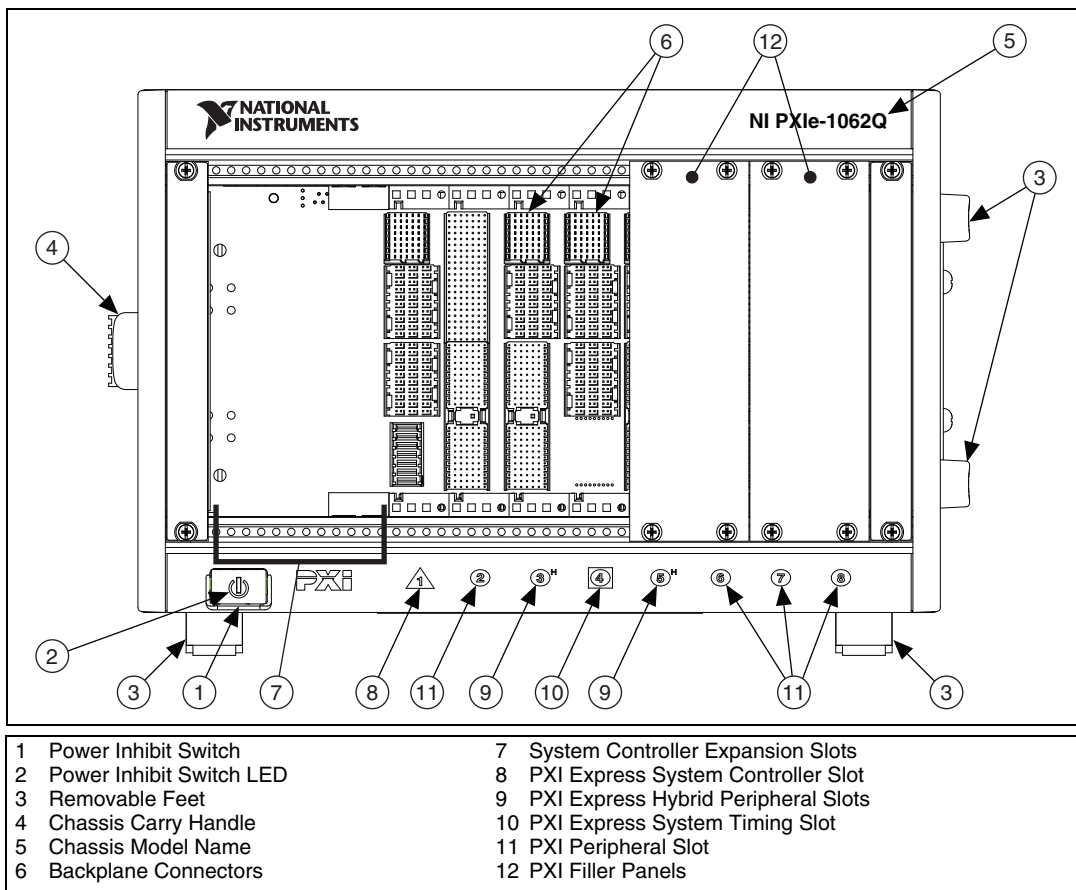
- PXI Express System Timing Slot for tight synchronization across chassis
- Rear CLK10 I/O connectors
- Switchless CLK10 routing

## **Optional Features**

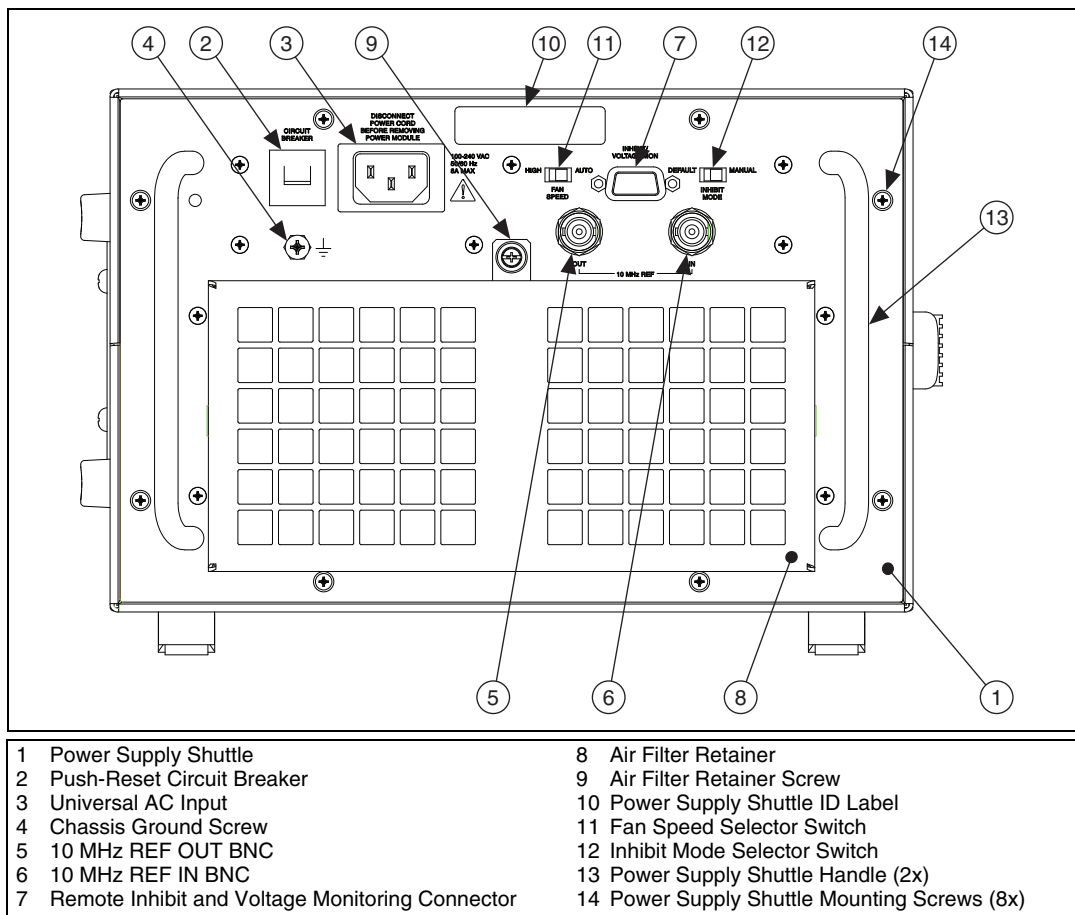
- Front and rear rack-mount kits
- Replacement power supply shuttle
- EMC filler panels
- Slot blockers for improved cooling performance
- Factory installation services

# Chassis Description

Figures 1-1 and 1-2 show the key features of the NI PXIe-1062Q chassis front and back panels. Figure 1-1 shows the front view of the NI PXIe-1062Q. Figure 1-2 shows the rear view of the NI PXIe-1062Q.



**Figure 1-1.** Front View of the NI PXIe-1062Q Chassis



**Figure 1-2.** Rear View of the NI PXIe-1062Q Chassis

## Optional Equipment

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Contact National Instruments to order the following options for the NI PXIe-1062Q chassis.

### EMC Filler Panels

Optional EMC filler panel kits are available from National Instruments.

### Rack Mount Kit

There are two optional kits for mounting the NI PXIe-1062Q chassis into a rack. The first option is a pair of mounting brackets for use on the front of the chassis. The second option is a rear rack mount kit. The rear rack mount kit differs from the front kit to allow for easier installation into the rack. For more information, refer to Figure A-3, [NI Chassis Rack Mount Kit Components](#).

### Slot Blockers

Optional slot blocker kits are available from National Instruments for improved thermal performance when all slots are not used.

## NI PXIe-1062Q Chassis Backplane Overview

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This section provides an overview of the backplane features for the NI PXIe-1062Q chassis.

### Interoperability with CompactPCI

The design of the NI PXIe-1062Q provides you the flexibility to use the following devices in a single PXI Express chassis:

- PXI Express compatible products
- CompactPCI Express compatible 4-Link system controller products
- CompactPCI Express compatible Type-2 peripheral products
- PXI peripheral products
- Standard CompactPCI peripheral products

## System Controller Slot

The system controller slot is Slot 1 of the chassis and is a 4-Link configuration system slot as defined by the CompactPCI Express and PXI Express specifications. It has three system controller expansion slots for system controller modules that are wider than one slot. These slots allow the system controller to expand to the left to prevent the system controller from using peripheral slots.

The backplane routes a x4 PCI Express link from the system controller slot to slots 3, 4, and 5, and a x1 PCI Express link to a PCI Express to PCI Translation Bridge on the backplane. The PCI Express to PCI Translation Bridge on the backplane provides a 32-bit/33MHz PCI bus to slots 2, 3, 5, 6, 7, and 8.

The system controller slot also has connectivity to some PXI features such as: PXI\_CLK10, PXI Star, PXI Trigger Bus and PXI Local Bus 6.

By default, the system controller will control the power supply with the PS\_ON# signals. A logic low on this line will turn the power supply on.



**Note** The Inhibit Mode switch on the rear of the chassis must be in the **Default** position for the system controller to have control of the power supply. Refer to the [Inhibit Mode Switch](#) section of Chapter 2, [Installation and Configuration](#), for details about the Inhibit Mode switch.

## Hybrid Peripheral Slots

The chassis provides two hybrid peripheral slots as defined by the *PXI-5 PXI Express Hardware Specification*: slot 3 and slot 5. A hybrid peripheral slot can accept the following peripheral modules:

- A PXI Express Peripheral with x4 or x1 PCI Express link to the system slot
- A CompactPCI Express Type-2 Peripheral with x4 or x1 PCI Express link to the system slot
- A hybrid-compatible PXI Peripheral module that has been modified by replacing the J2 connector with an XJ4 connector installed in the upper eight rows of J2. Refer to the *PXI Express Specification* for details. The PXI Peripheral communicates through the backplane's 32-bit PCI bus.
- A CompactPCI 32-bit peripheral on the backplane's 32-bit PCI bus

The hybrid peripheral slots provide full PXI Express functionality and 32-bit PXI functionality except for PXI Local Bus. The hybrid peripheral slot only connects to PXI Local Bus 6 left and right.

## PXI Peripheral Slots

There are four PXI peripheral slots which will accept PXI or CompactPCI peripherals: slot 2, slot 6, slot 7, and slot 8. These slots are on the backplane's 32-bit PCI bus. These slots offer full PXI functionality, but have no PXI Express features. The 64-bit PCI signals on the P2 connectors are not connected.

## System Timing Slot

The System Timing Slot is slot 4. The system timing slot will accept the following peripheral modules:

- A PXI Express System Timing Module with x4 or x1 PCI Express link to the system slot.
- A PXI Express Peripheral with x4 or x1 PCI Express link to the system slot.
- A CompactPCI Express Type-2 Peripheral with x4 or x1 PCI Express link to the system slot.

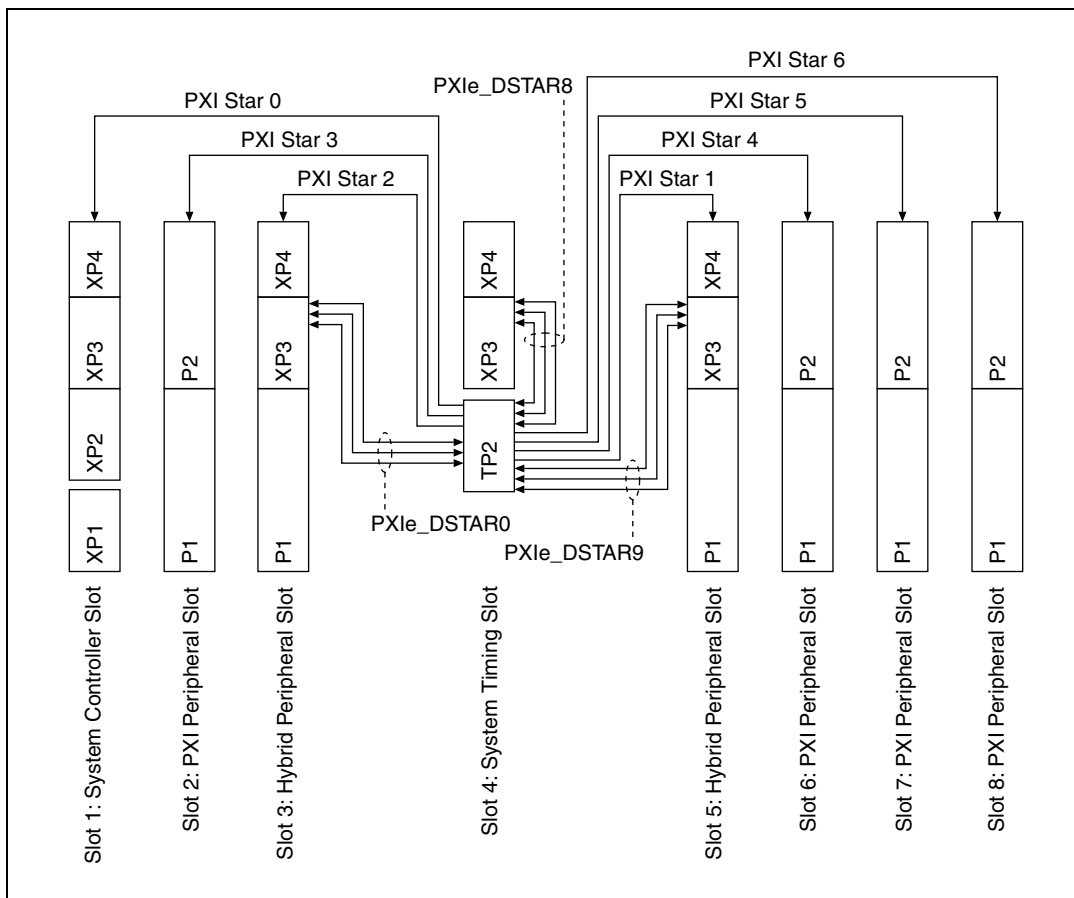
The system timing slot has 3 dedicated differential pairs (PXIe\_DSTAR) connected from the TP2 connector to the XP3 connector for each hybrid peripheral slot, as well as routed back to the XP3 connector of the system timing slot as shown in Figure 1-3. The PXIe\_DSTAR pairs can be used for high-speed triggering, synchronization and clocking. Refer to the *PXI Express Specification* for details.

The system timing slot also has a single-ended (PXI Star) trigger connected to every slot. Refer to Figure 1-3 for details.

The system timing slot has a pin (PXI\_CLK10\_IN) through which a system timing module may source a 10MHz clock to which the backplane will phase-lock. Refer to the [System Reference Clock](#) section for details.

The system timing slot has a pin (PXIe\_SYNC\_CTRL) through which a system timing module can control the PXIe\_SYNC100 timing. Refer to the *PXI Express Specification* and the [PXIe\\_SYNC\\_CTRL](#) section of this chapter for details.





**Figure 1-3.** PXIe\_DSTAR and PXI Star Connectivity Diagram

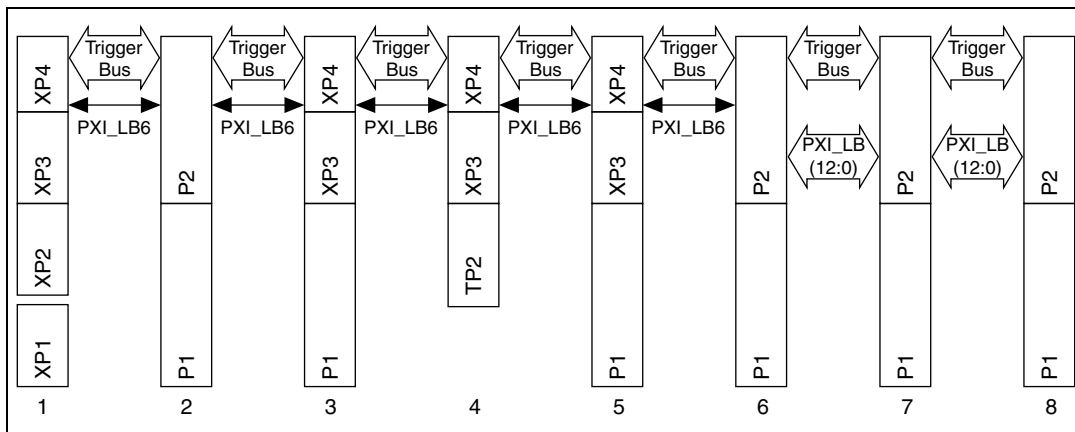
## PXI Local Bus

The PXI backplane local bus is a daisy-chained bus that connects each peripheral slot with adjacent peripheral slots to the left and right, as shown in Figure 1-4.

The backplane routes the full 13-line PXI Local Bus between adjacent PXI slots (slots 6, 7, and 8) and PXI Local Bus 6 between all other slots. Refer to Figure 1-4 for details. The left local bus 6 from slot 1 is not routed anywhere and the right local bus signals from slot 8 are not routed anywhere.

Local bus signals may range from high-speed TTL signals to analog signals as high as 42 V.

Initialization software uses the configuration information specific to each adjacent peripheral module to evaluate local bus compatibility.



**Figure 1-4.** PXI Trigger Bus and Local Bus Connectivity Diagram

## PXI Trigger Bus

All slots share eight trigger lines. You can use these trigger lines in a variety of ways. For example, you can use triggers to synchronize the operation of several different PXI peripheral modules. In other applications, one module can control carefully timed sequences of operations performed on other modules in the system. Modules can pass triggers to one another, allowing precisely timed responses to asynchronous external events the system is monitoring or controlling.

## System Reference Clock

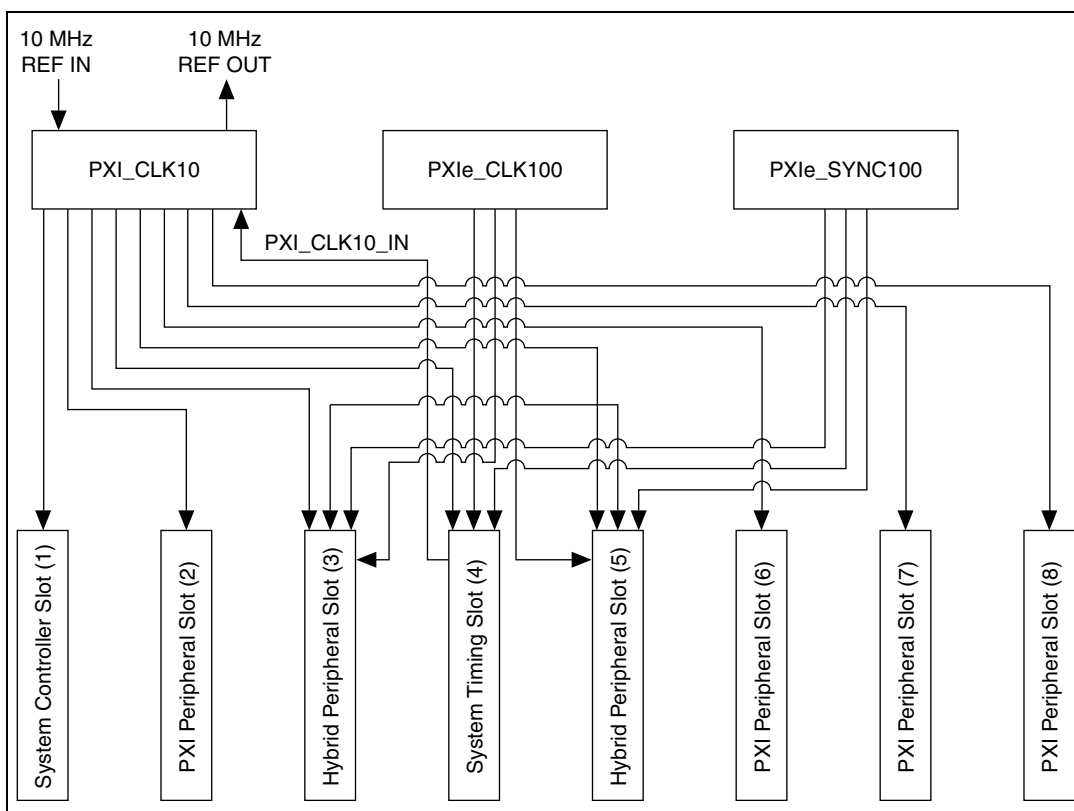
The NI PXIe-1062Q chassis supplies the PXI 10 MHz system clock signal (PXI\_CLK10) independently driven to each peripheral slot and PXIe\_CLK100 and PXIe\_SYNC100 to the hybrid slots and system timing slot.

An independent buffer (having a source impedance matched to the backplane and a skew of less than 250 ps between slots) drives PXI\_CLK10 to each peripheral slot. Refer to Figure 1-5 for the routing configuration of PXI\_CLK10. You can use this common reference clock signal to synchronize multiple modules in a measurement or control system.

An independent buffer drives PXIe\_CLK100 to the hybrid peripheral slots and system timing slot. Refer to Figure 1-5 for the routing configuration of PXIe\_CLK100. These clocks are matched in skew to less than 100 ps. The

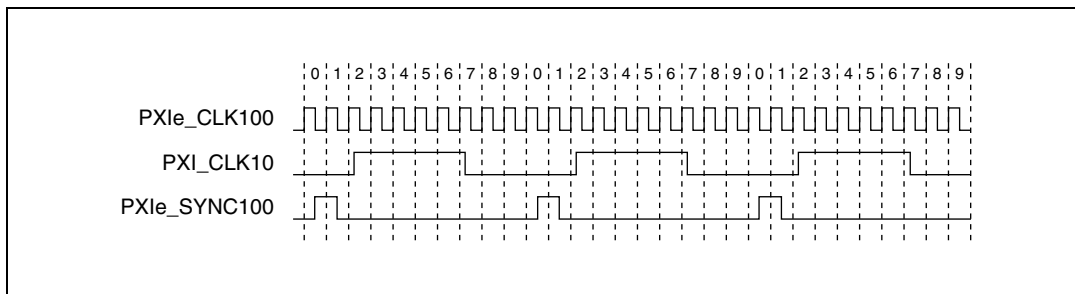
differential pair must be terminated on the peripheral with LVPECL termination for the buffer to drive PXIe\_CLK100 so that when there is no peripheral or a peripheral that does not connect to PXIe\_CLK100, there is no clock being driven on the pair to that slot.

An independent buffer drives PXIe\_SYNC100 to the hybrid peripheral slot and system timing slot. Refer to Figure 1-5 for the routing configuration of PXIe\_SYNC100. These clocks are matched in skew to less than 100 ps. The differential pair must be terminated on the peripheral with LVPECL termination for the buffer to drive PXIe\_SYNC100 so that when there is no peripheral or a peripheral that does not connect to PXIe\_SYNC100, there is no clock being driven on the pair to that slot.



**Figure 1-5.** Distribution of PXI\_CLK10, PXIe\_CLK100, and PXIe\_SYNC100

PXI\_CLK10, PXIe\_CLK100 and PXIe\_SYNC100 have the default timing relationship described in Figure 1-6.



**Figure 1-6.** System Reference Clock Default Behavior

To synchronize the system to an external clock, you can drive PXI\_CLK10 from an external source through the PXI\_CLK10\_IN pin on the System Timing Slot. Refer to Table B-7, [XP4 Connector Pinout for the System Timing Slot](#), for the pinout. When a 10 MHz clock is detected on this pin, the backplane automatically phase-locks the PXI\_CLK10, PXIe\_CLK100, and PXIe\_SYNC100 signals to this external clock and distributes these signals to the slots (refer to Figure 1-5 for the distribution of PXI\_CLK10, PXIe\_CLK100 and PXIe\_SYNC100). Refer to Appendix A, [Specifications](#), for the specification information for an external clock provided on the PXI\_CLK10\_IN pin of the system timing slot.

You also can drive a 10 MHz clock on the 10 MHz REF IN connector on the rear of the chassis. When a 10 MHz clock is detected on this connector, the backplane automatically phase-locks the PXI\_CLK10, PXIe\_CLK100, and PXIe\_SYNC100 signals to this external clock and distributes these signals to the slots (refer to Figure 1-5 for the distribution of PXI\_CLK10, PXIe\_CLK100 and PXIe\_SYNC100). Refer to Appendix A, [Specifications](#), for the specification information for an external clock provided on the 10 MHz REF IN connector on the rear panel of the chassis.

If the 10 MHz clock is present on both the PXI\_CLK10\_IN pin of the System Timing Slot and the 10 MHz REF IN connector on the rear of the chassis, the signal on the System Timing Slot is selected. Refer to Table 1-2 which explains how the 10 MHz clocks are selected by the backplane.

**Table 1-2.** Backplane External Clock Input Truth Table

| System Timing Slot<br>PXI_CLK10_IN | Rear Chassis Panel<br>10 MHz REF IN | Backplane PXI_CLK10,<br>PXIe_CLK100 and PXIe_SYNC100                                         |
|------------------------------------|-------------------------------------|----------------------------------------------------------------------------------------------|
| No clock present                   | No clock present                    | Backplane generates its own clocks                                                           |
| No clock present                   | 10 MHz clock present                | PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 all phase-locked to Rear Chassis Panel—10 MHz REF IN |
| 10 MHz clock present               | No clock present                    | PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 all phase-locked to System Timing Slot—PXI_CLK10_IN  |
| 10 MHz clock present               | 10MHz clock present                 | PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 all phase-locked to System Timing Slot—PXI_CLK10_IN  |

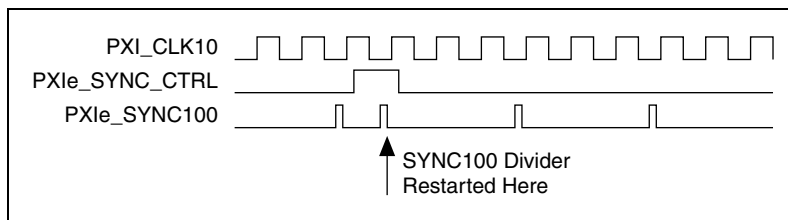
A copy of the backplane's PXI\_CLK10 is exported to the 10 MHz REF OUT connector on the rear of the chassis. This clock is driven by an independent buffer. Refer to Appendix A, [Specifications](#), for the specification information for the 10 MHz REF OUT signal on the rear panel of the chassis.

## PXIe\_SYNC\_CTRL

PXIe\_SYNC100 is by default a 10 ns pulse synchronous to PXI\_CLK10. The frequency of PXIe\_SYNC100 is  $10/n$  MHz, where  $n$  is a positive integer. The default for  $n$  is 1, giving PXIe\_SYNC100 a 100 ns period. However, the backplane allows  $n$  to be programmed to other integers. For instance, setting  $n = 3$  gives a PXIe\_SYNC100 with a 300 ns period while still maintaining its phase relationship to PXI\_CLK10. The value for  $n$  may be set to any positive integer from 1 to 255.

The system timing slot has a control pin for PXIe\_SYNC100 called PXIe\_SYNC\_CTRL for use when  $n > 1$ . Refer to Table B-6, [XP3 Connector Pinout for the System Timing Slot](#), for system timing slot pinout. Refer to Appendix A, [Specifications](#), for the PXIe\_SYNC\_CTRL input specifications.

By default, a high-level detected by the backplane on the PXIe\_SYNC\_CTRL pin causes a synchronous restart for the PXIe\_SYNC100 signal. On the next PXI\_CLK10 edge the PXIe\_SYNC100 signal will restart. This will allow several chassis to have their PXIe\_SYNC100 in phase with each other. Refer to Figure 1-7 for timing details with this method.



**Figure 1-7.** PXIe\_SYNC100 at 3.33 MHz Using PXIe\_SYNC\_CTRL as Restart

---

# Installation and Configuration

This chapter describes how to prepare and operate the NI PXIe-1062Q chassis.

Before connecting the chassis to a power source, read this chapter and the *Read Me First: Safety and Electromagnetic Compatibility* document included with your kit.

## Safety Information

---



**Caution** Before undertaking any troubleshooting, maintenance, or exploratory procedure, carefully read the following caution notices.

This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.

- **Chassis Grounding**—The chassis requires a connection from the premise wire safety ground to the chassis ground. The earth safety ground must be connected during use of this equipment to minimize shock hazards. Refer to the [Connecting Safety Ground](#) section for instructions on connecting safety ground.
- **Live Circuits**—Operating personnel and service personnel *must* not remove protective covers when operating or servicing the chassis. Adjustments and service to internal components must be undertaken by qualified service technicians. During service of this product, the mains connector to the premise wiring must be disconnected. Dangerous voltages may be present under certain conditions; use extreme caution.
- **Explosive Atmosphere**—Do *not* operate the chassis in conditions where flammable gases are present. Under such conditions, this equipment is unsafe and may ignite the gases or gas fumes.

- **Part Replacement**—Only service this equipment with parts that are exact replacements, both electrically and mechanically. Contact National Instruments for replacement part information. Installation of parts with those that are not direct replacements may cause harm to personnel operating the chassis. Furthermore, damage or fire may occur if replacement parts are unsuitable.
- **Modification**—Do *not* modify any part of the chassis from its original condition. Unsuitable modifications may result in safety hazards.

## Chassis Cooling Considerations

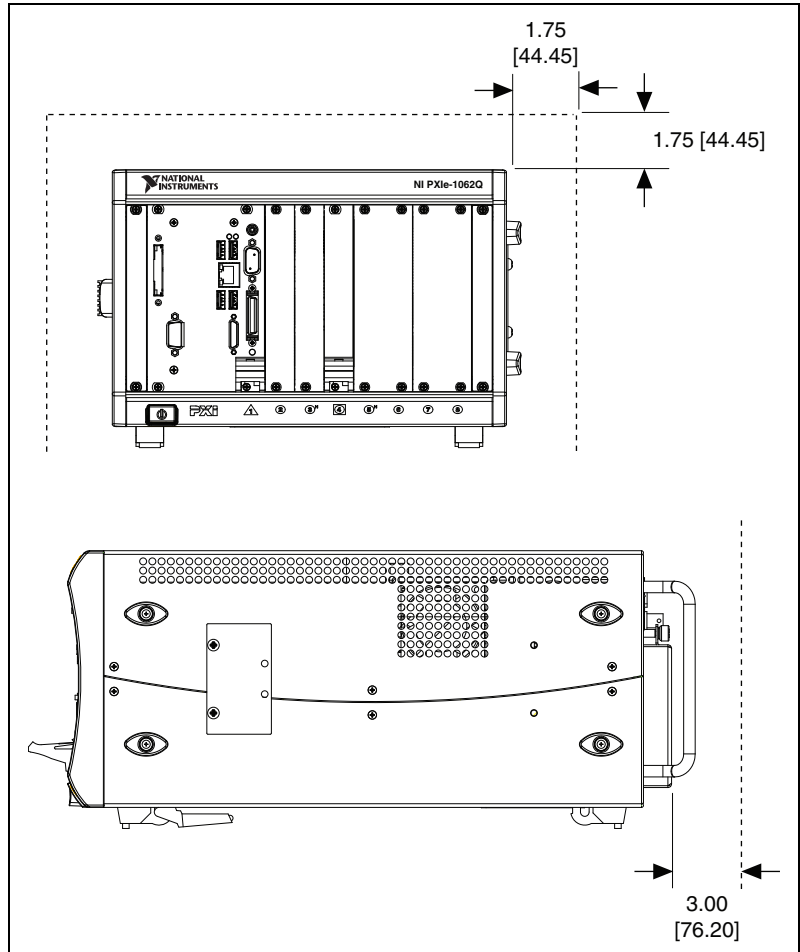
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The NI PXIe-1062Q chassis is designed to operate on a bench or in an instrument rack. Regardless of the configuration you must provide the cooling clearances as outlined in the following sections.

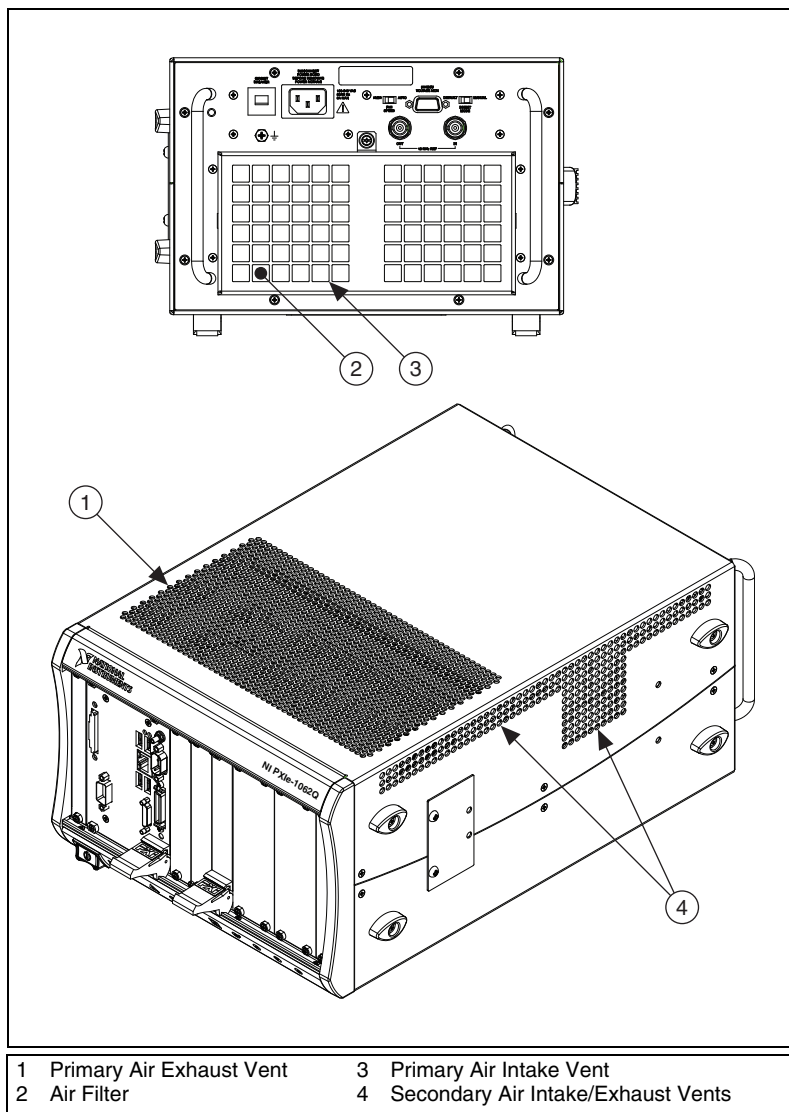
### Providing Adequate Clearance

The primary cooling exhaust vent for the NI PXIe-1062Q is on the top of the chassis. The primary intake vent is on the rear of the chassis where the air is filtered as it enters the power supply shuttle. The secondary intake and exhaust vents are located along the sides of the chassis. Adequate clearance between the chassis and surrounding equipment or blockages must be maintained to ensure proper cooling of the chassis power supply as well as the modules plugged into the chassis. These clearances are outlined in Figure 2-1. The vent locations for the NI PXIe-1062Q chassis are shown in Figure 2-2. Failure to provide these clearances may result in thermal-related failures in the chassis or modules.





**Figure 2-1.** NI PXIe-1062Q Cooling Clearances



**Figure 2-2.** NI PXIe-1062Q Vents

## Chassis Ambient Temperature Definition

The chassis fan control system uses intake air temperature as the input for controlling fan speeds when in Auto Fan Speed mode. Because of this, the chassis ambient temperature is defined as the temperature that exists just outside of the fan intake vents on the rear of the chassis. Note that this temperature may be higher than ambient room temperature depending on the surrounding equipment and/or blockages present. It is the user's responsibility to ensure that this ambient temperature does not exceed the rated ambient temperature as stated in Appendix A, [Specifications](#). If the temperature exceeds the stated spec the power switch LED will blink green, as discussed in the [Power Inhibit Switch LED Indicator](#) section of this chapter.

## Setting Fan Speed

The fan-speed selector switch is on the rear panel of the NI PXIe-1062Q chassis. Refer to Figure 1-2, [Rear View of the NI PXIe-1062Q Chassis](#), to locate the fan-speed selector switch. Select **High** for maximum cooling performance or **Auto** for improved acoustic performance. When set to **Auto**, the fan speed is determined by chassis intake air temperature.

## Installing Filler Panels

To maintain proper module cooling performance, install filler panels (provided with the chassis) in unused or empty slots. Secure with the captive mounting screws provided.

## Installing Slot Blockers

The cooling performance of the chassis can be improved by installing optional slot blockers. Refer to [ni.com](http://ni.com) for more details.

## Rack Mounting

---

Rack mount applications require the optional rack mount kits available from National Instruments. Refer to the instructions supplied with the rack mount kits to install your NI PXIe-1062Q chassis in an instrument rack. Refer to Figure A-3, [NI Chassis Rack Mount Kit Components](#).



**Note** You may want to remove the feet from the NI PXIe-1062Q chassis when rack mounting. To do so, remove the screws holding the feet in place.

## Connecting Safety Ground

---



**Caution** The NI PXIe-1062Q chassis are designed with a three-position NEMA 5-15 style plug for the U.S. that connects the ground line to the chassis ground. To minimize shock hazard, make sure the electrical power outlet you use to power the chassis has an appropriate earth safety ground.

If your power outlet does not have an appropriate ground connection, you must connect the premise safety ground to the chassis grounding screw located on the rear panel. Refer to Figure 1-2, [Rear View of the NI PXIe-1062Q Chassis](#), to locate the chassis grounding screw. To connect the safety ground, complete the following steps:

1. Connect a 16 AWG (1.3 mm) wire to the chassis grounding screw using a grounding lug. The wire must have green insulation with a yellow stripe or must be noninsulated (bare).
2. Attach the opposite end of the wire to permanent earth ground using toothed washers or a toothed lug.

## Connecting to Power Source

---



**Cautions** Do *not* install modules prior to performing the following power-on test.

To completely remove power, you *must* disconnect the AC power cable.

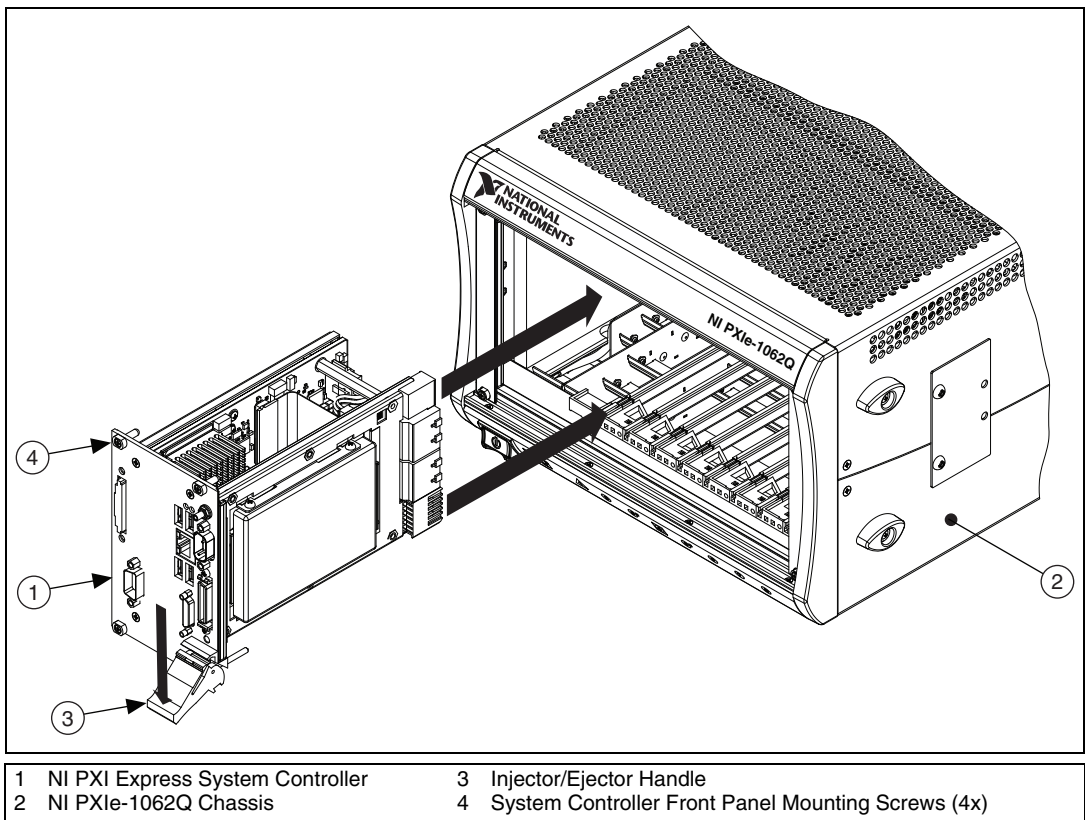
Attach input power through the rear AC inlet using the appropriate AC power cable supplied. Refer to Figure 1-2, [Rear View of the NI PXIe-1062Q Chassis](#), to locate the AC inlet.

The Inhibit Mode switch allows you to power on the chassis or place it in standby mode. Set the Inhibit Mode switch on the back of the chassis to the **Manual** position. Observe that all fans become operational and the power switch LED is a steady green. Switching the Inhibit Mode switch to the **Default** position allows the system controller to control the power supply.

# Installing a PXI Express System Controller

This section contains general installation instructions for installing a PXI Express system controller in a NI PXIe-1062Q chassis. Refer to your PXI Express system controller user manual for specific instructions and warnings. To install a system controller, complete the following steps:

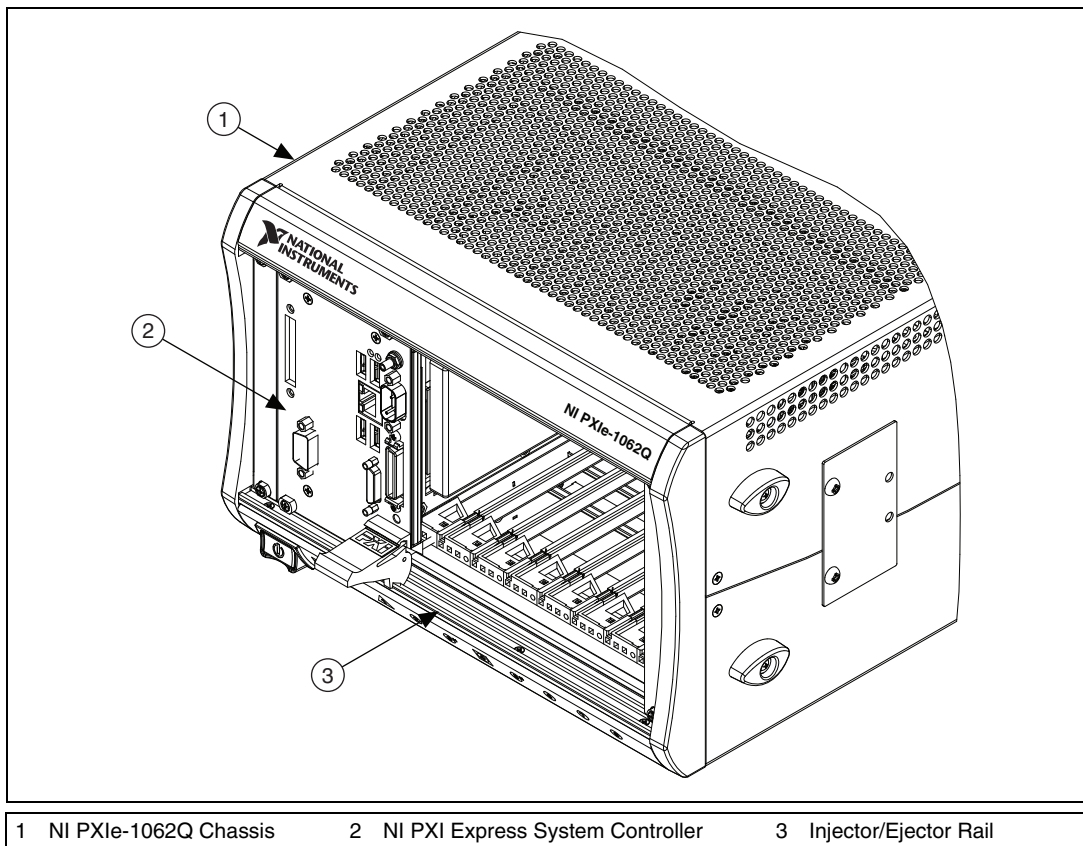
1. Connect the AC power source to the PXI Express chassis before installing the system controller. The AC power cord grounds the chassis and protects it from electrical damage while you install the system controller.
2. Install the system controller into the system controller slot (slot 1, indicated by the red card guides) by first placing the system controller PCB into the front of the card guides (top and bottom). Slide the system controller to the rear of the chassis, making sure that the injector/ejector handle is pushed down as shown in Figure 2-3.



**Figure 2-3.** Installing a PXI Express System Controller

3. When you begin to feel resistance, push up on the injector/ejector handle to seat the system controller fully into the chassis frame. Secure the system controller front panel to the chassis using the system controller front-panel mounting screws.
4. Connect the keyboard, mouse, and monitor to the appropriate connectors. Connect devices to ports as required by your system configuration.
5. Power on the chassis. Verify that the system controller boots. If the system controller does not boot, refer to your system controller user manual.

Figure 2-4 shows a PXI Express system controller installed in the system controller slot of a NI PXIe-1062Q chassis. You can place CompactPCI, CompactPCI Express, PXI, or PXI Express modules in other slots depending on the slot type.



**Figure 2-4.** NI PXI Express System Controller Installed in a NI PXIe-1062Q Chassis

# Installing Peripheral Modules

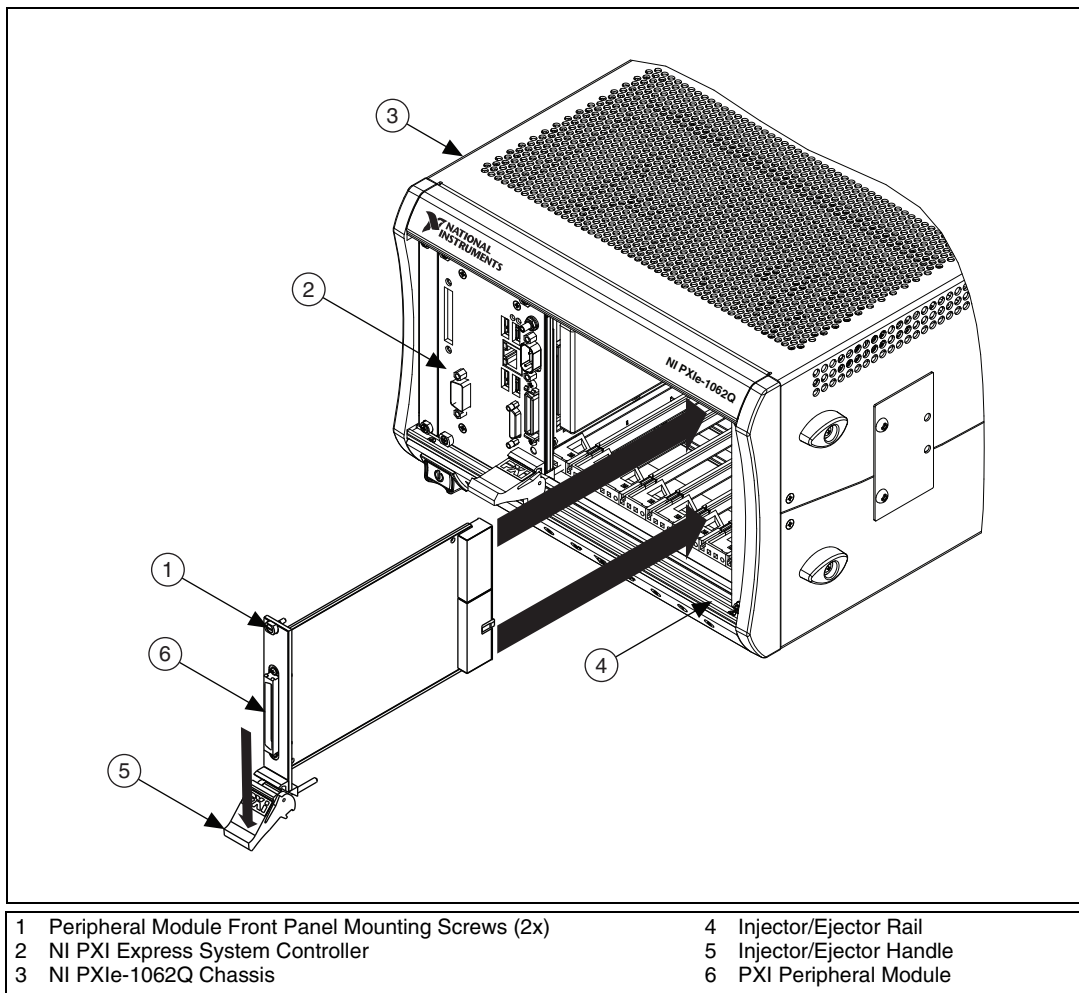
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**Caution** The NI PXIe-1062Q chassis has been designed to accept a variety of peripheral module types in different slots. To prevent damage to the chassis, ensure that the peripheral module is being installed into a slot designed to accept it. Refer to Chapter 1, [Getting Started](#), for a description of the various slot types.

This section contains general installation instructions for installing a peripheral module in a NI PXIe-1062Q chassis. Refer to your peripheral module user manual for specific instructions and warnings. To install a module, complete the following steps:

1. Connect the AC power source to the PXI Express chassis before installing the module. The AC power cord grounds the chassis and protects it from electrical damage while you install the module.
2. Ensure that the chassis is powered off.
3. Install a module into a chassis slot by first placing the module card PCB into the front of the card guides (top and bottom), as shown in Figure 2-5. Slide the module to the rear of the chassis, making sure that the injector/ejector handle is pushed down as shown in Figure 2-5.
4. When you begin to feel resistance, push up on the injector/ejector handle to fully seat the module into the chassis frame. Secure the module front panel to the chassis using the module front-panel mounting screws.



**Figure 2-5.** Installing PXI, PXI Express, or CompactPCI Peripheral Modules

## Power Inhibit Switch LED Indicator

The chassis power inhibit switch has an integrated LED. This LED indicates one of four different conditions:

- If the inhibit switch LED is steady green (not flashing), the chassis is powered on and operating normally.
- If the inhibit switch LED is flashing green, the air-intake temperature has exceeded the chassis operating range.



- If the inhibit switch LED is flashing red, the power supply outputs are not within voltage regulation requirements.
- If the inhibit switch LED is steady red, the system fans or power supply fan has failed. The remaining fans will automatically be driven high.



**Note** If both system fans or the power supply fan fails the chassis will shut down automatically, preventing the chassis and modules from damage due to overheating.

# Remote Voltage Monitoring and Control

The NI PXIe-1062Q chassis supports remote voltage monitoring and inhibiting through a female 9-pin D-SUB (DB-9) connector located on the rear panel. Table 2-1 shows the pinout of the 9-pin D-SUB (DB-9) connector.

**Table 2-1.** Remote Inhibit and Voltage Monitoring Connector Pinout

| DB-9 Pin | Signal               |
|----------|----------------------|
| 1        | Logic Ground         |
| 2        | +5 VDC               |
| 3        | Reserved             |
| 4        | +3.3 VDC             |
| 5        | Inhibit (Active Low) |
| 6        | +12 VDC              |
| 7        | Reserved             |
| 8        | –12 VDC              |
| 9        | Logic Ground         |



**Caution** When connecting digital voltmeter probes to the rear 9-pin D-SUB (DB-9) connector, be careful not to short the probe leads together. Doing so could damage the power supply.

You can use a digital voltmeter to ensure all voltage levels in the NI PXIe-1062Q chassis are within the allowable limits. Referring to Table 2-2, connect one lead of the voltmeter to a supply pin on the remote voltage monitoring connector (9-pin D-SUB) on the rear panel. Refer to Table 2-1 for a pinout diagram of the remote voltage monitoring connector. Connect the reference lead of the voltmeter to one of the ground pins. Compare each voltage reading to the values listed in Table 2-2.



**Note** Use the rear-panel 9-pin D-SUB connector to check voltages only. Do not use the connector to supply power to external devices.

**Table 2-2.** Power Supply Voltages at Voltage Monitoring Connector (DB-9)

| Pin  | Supply       | Acceptable Voltage Range |
|------|--------------|--------------------------|
| 2    | +5 V         | 4.75 to 5.25 V           |
| 4    | +3.3 V       | 3.135 to 3.465 V         |
| 6    | +12 V        | 11.4 to 12.6 V           |
| 8    | –12 V        | –12.6 to –11.4 V         |
| 1, 9 | Logic Ground | 0 V                      |

If the voltages fall within the specified ranges, the chassis complies with the CompactPCI voltage-limit specifications.

## Inhibit Mode Switch

---

On the rear panel of the chassis there is an Inhibit Mode switch. Refer to Figure 1-2, [Rear View of the NI PXIe-1062Q Chassis](#), for the location. The Inhibit Mode switch is recessed to prevent it from accidentally being switched.

The Inhibit Mode switch should be in the **Default** position when normal power inhibit switch functionality is desired. If the user needs to power on a chassis without a system controller installed the switch should be in the **Manual** position.

When the Inhibit Mode switch is set to the **Manual** position, the power supplies are enabled, and you can use the Inhibit signal (active low) on pin 5 of the Remote Inhibit and Voltage Monitoring connector to power off the chassis. To remotely power off the chassis, connect the Inhibit pin (pin 5) to a Logic Ground pin (pin 1 or 9). As long as this connection exists, the chassis will remain off (standby); when you remove this connection, the chassis turns on.



**Note** For the Remote Inhibit signal to control the On/Off (standby) state of the chassis, the Inhibit Mode switch must be in the **Manual** position.

## PXI\_CLK10 Rear Connectors

---

There are two BNC connectors on the rear of the NI PXIe-1062Q chassis for PXI\_CLK10. The connectors are labeled IN and OUT. You can use them for supplying the backplane with PXI\_CLK10 or routing the backplane's PXI\_CLK10 to another chassis. Refer to the [System Reference Clock](#) section of Chapter 1, [Getting Started](#), for details about these signals.

# PXI Express System Configuration with MAX

The PXI Platform Services software included with your chassis automatically identifies your PXI Express system components to generate a `pxiesys.ini` file. You can configure your entire PXI system and identify PXI-1 chassis through Measurement & Automation Explorer (MAX), included with your system controller. MAX creates the `pxiesys.ini` and `pxisys.ini` file, which define your PXI system parameters. MAX also provides an interface to route and reserve triggers so dynamic routing, through drivers such as DAQmx, avoids double-driving and potentially damaging trigger lines. For more information about routing and reserving PXI triggers, refer to KnowledgeBase **3TJDOND8** at [ni.com/support](http://ni.com/support).

The configuration steps for single or multiple-chassis systems are the same.

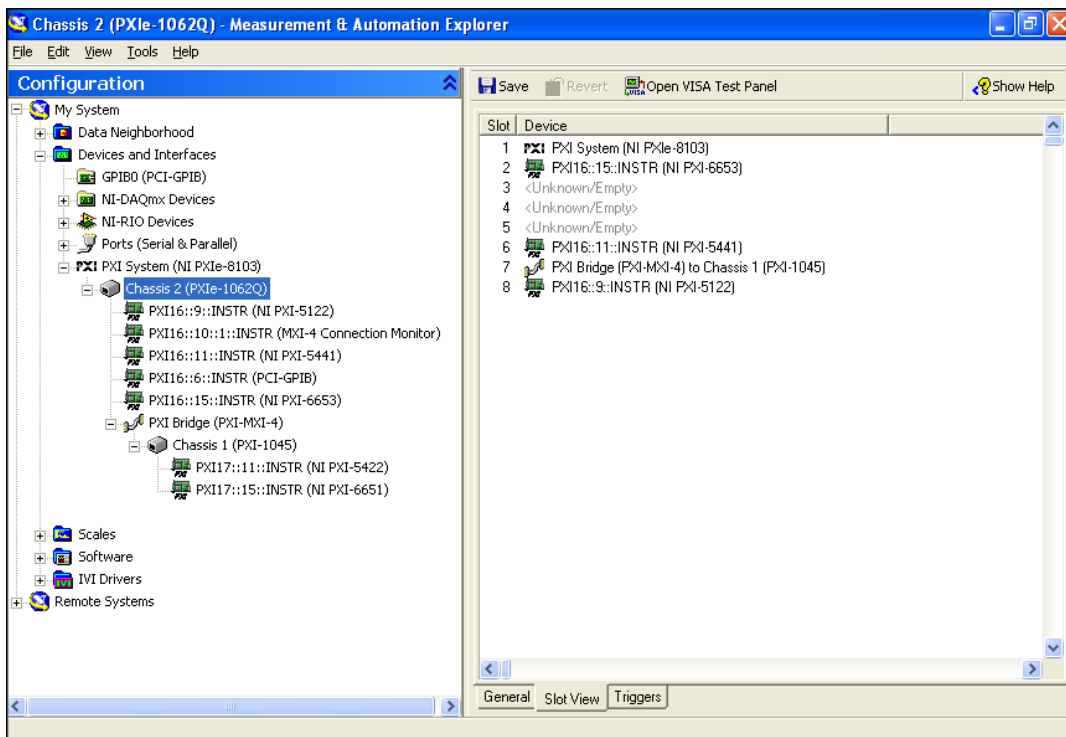


Figure 2-6. Multichassis Configuration in MAX

## PXI-1 System Configuration

1. Launch MAX.
2. In the **Configuration** tree, click the **Devices and Interfaces** branch to expand it.
3. If the PXI system controller has not yet been configured, it is labeled **PXI System (Unidentified)**. Right-click this entry to display the pop-up menu, then select the appropriate system controller model from the **Identify As** submenu.
4. Click the PXI system controller. The chassis (or multiple chassis, in a multichassis configuration) is listed below it. Identify each chassis by right-clicking its entry, then selecting the appropriate chassis model through the **Identify As** submenu. Further expanding the **PXI System** branch shows all devices in the system that can be recognized by NI-VISA. When your system controller and all your chassis are identified, the required `pxisys.ini` file is complete.

The PXI specification allows for many combinations of PXI chassis and system modules. To assist system integrators, the manufacturers of PXI chassis and system modules must document the capabilities of their products. PXI Express devices must provide a driver and `.ini` file for identification. These files are provided as part of the PXI Platform Services software included with your system controller. The minimum documentation requirements for PXI-1 are contained in `.ini` files, which consist of ASCII text. System integrators, configuration utilities, and device drivers can use these `.ini` files.

The capability documentation for a PXI-1 chassis is contained in a `chassis.ini` file provided by the chassis manufacturer. The information in this file is combined with information about the system controller to create a single PXI-1 system initialization file called `pxisys.ini` (PXI System Initialization). The NI system controller uses MAX to generate the `pxisys.ini` file from the `chassis.ini` file.

Device drivers and other utility software read the `pxiesys.ini` and `pxisys.ini` file to obtain system information. For detailed information about initialization files, refer to the PXI specification at [www.pxisa.org](http://www.pxisa.org).

## Using System Configuration and Initialization Files

---

The PXI Express specification allows many combinations of PXI Express chassis and system modules. To assist system integrators, the manufacturers of PXI Express chassis and system modules must document the capabilities of their products. The minimum documentation requirements are contained in `.ini` files, which consist of ASCII text. System integrators, configuration utilities, and device drivers can use these `.ini` files.

The capability documentation for the NI PXIe-1062Q chassis is contained in the `chassis.ini` file on the software media that comes with the chassis. The information in this file is combined with information about the system controller to create a single system initialization file called `pxisys.ini` (PXI System Initialization). The system controller manufacturer either provides a `pxisys.ini` file for the particular chassis model that contains the system controller or provides a utility that can read an arbitrary `chassis.ini` file and generate the corresponding `pxisys.ini` file. System controllers from NI provide the `pxisys.ini` file for the NI PXIe-1062Q chassis, so you should not need to use the `chassis.ini` file. Refer to the documentation provided with the system controller or to [ni.com/support](http://ni.com/support) for more information on `pxisys.ini` and `chassis.ini` files.

Device drivers and other utility software read the `pxisys.ini` file to obtain system information. The device drivers should have no need to directly read the `chassis.ini` file. For detailed information regarding initialization files, refer to the PXI Express specification at [www.pxisa.org](http://www.pxisa.org).

---

# Maintenance

This chapter describes basic maintenance procedures you can perform on the NI PXIe-1062Q chassis.



**Caution** Disconnect the power cable prior to servicing a NI PXIe-1062Q chassis.

---

## Service Interval

Clean the chassis fan filters at a maximum interval of six months. Depending on the amount of use and ambient dust levels in the operating environment, the filters may require more frequent cleaning.

Clean dust from the chassis exterior (and interior) as needed, based on the operating environment. Periodic cleaning increases reliability.

---

## Preparation

The information in this section is designed for use by qualified service personnel. Read the *Read Me First: Safety and Electromagnetic Compatibility* document included with your kit before attempting any procedures in this chapter.



**Caution** Many components within the chassis are susceptible to static discharge damage. Service the chassis only in a static-free environment. Observe standard handling precautions for static-sensitive devices while servicing the chassis. Always wear a grounded wrist strap or equivalent while servicing the chassis.

---

## Cleaning

Cleaning procedures consist of exterior and interior cleaning of the chassis and cleaning the fan filters. Refer to your module user documentation for information on cleaning the individual CompactPCI or PXI Express modules.



**Caution** Always disconnect the AC power cable before cleaning or servicing the chassis.

## Interior Cleaning

Use a dry, low-velocity stream of air to clean the interior of the chassis.  
Use a soft-bristle brush for cleaning around components.

## Exterior Cleaning

Clean the exterior surfaces of the chassis with a dry lint-free cloth or a soft-bristle brush. If any dirt remains, wipe with a cloth moistened in a mild soap solution. Remove any soap residue by wiping with a cloth moistened with clear water. Do not use abrasive compounds on any part of the chassis.



**Caution** Avoid getting moisture inside the chassis during exterior cleaning, especially through the top vents. Use just enough moisture to dampen the cloth.

Do *not* wash the front- or rear-panel connectors or switches. Cover these components while cleaning the chassis.

Do *not* use harsh chemical cleaning agents; they may damage the chassis. Avoid chemicals that contain benzene, toluene, xylene, acetone, or similar solvents.

## Cleaning the Fan Filters

---

Dirty fan filters can dramatically affect the cooling performance of a NI PXIe-1062Q chassis. Clean the filters whenever they become visibly dirty. You can easily remove the chassis air filters from the rear of the chassis by removing the filter retainer. To remove the filter retainer, loosen the retainer screw. The filter cover and retainer are shown in Figure 1-2, [Rear View of the NI PXIe-1062Q Chassis](#).

Clean the fan filters by washing them in a mild soap solution and then vacuuming or blowing air through them. Rinse the filters with water and allow them to dry before reinstalling them on the chassis.

## Resetting the AC Mains Circuit Breaker

---

If the NI PXIe-1062Q chassis is connected to an AC source and encounters an over-current condition, the circuit breaker on the rear panel will trip to prevent damage to the chassis. Complete the following steps to reset the circuit breaker.

1. Turn off the chassis.
2. Disconnect the AC power cable.



3. Depress the circuit breaker to reset it.
4. Reconnect the AC power cable.
5. Turn on the chassis.

If the circuit breaker trips again, complete the following steps:

1. Turn off the chassis.
2. Disconnect the AC power cable.
3. Remove all modules from the chassis.
4. Complete the procedure described in the [Connecting to Power Source](#) section of Chapter 2, [Installation and Configuration](#). If the power switch LED is not a steady green, contact National Instruments.
5. Verify that the NI PXIe-1062Q chassis can meet the power requirements of your CompactPCI or PXI Express modules. Overloading the chassis can cause the breaker to trip. Refer to Appendix A, [Specifications](#).
6. The over-current condition that caused the circuit breaker to trip may be due to a faulty CompactPCI or PXI Express module. Refer to the documentation supplied with the modules for troubleshooting information.

## Replacing the Modular Power Supply

---

This section describes how to remove, configure, and install the AC power supply shuttle in the NI PXIe-1062Q chassis.



**Cautions** Disconnect the power cable prior to replacing the power supply.

Do not attempt to use a power supply shuttle from another chassis such as the NI PXI-1042. Doing so may damage your chassis and the power supply shuttle.

Before connecting the power supply shuttle to a power source, read this section and the *Read Me First: Safety and Electromagnetic Compatibility* document included with the kit.

## Removal

The NI PXIe-1062Q AC power supply is a replacement part for the NI PXIe-1062Q AC chassis. Before attempting to replace the power supply shuttle, verify that there is adequate clearance behind the chassis. Disconnect the power cable from the power supply shuttle on the back of the chassis. Identify the eight mounting screws for the NI PXIe-1062Q that

attach the power supply shuttle to the chassis. Refer to Figure 1-2, [Rear View of the NI PXIe-1062Q Chassis](#), for the screw locations. Using a Phillips screwdriver, remove the screws. Pull on the two rear handles of the power supply shuttle to remove it from the back of the chassis.

## Installation

Ensure that there is no visible damage to the new power supply shuttle. Verify that the housing and connector on the new power supply shuttle have no foreign material inside. Remove the protective cap on the PXI\_CLK10 connector. Install the new power supply shuttle into the opening on the rear of the chassis. Replace and tighten the eight screws with a Phillips screwdriver.

## Configuration

The fan-speed selector switch is on the rear panel of the power supply shuttle. Refer to Figure 1-2, [Rear View of the NI PXIe-1062Q Chassis](#), to locate the fan-speed selector. Select **High** for maximum cooling performance (recommended) or **Auto** for quieter operation. Set the Inhibit Mode switch to the **Default** position.

## Connecting Safety Ground

Refer to the [Connecting Safety Ground](#) section of Chapter 2, [Installation and Configuration](#).

## Connecting to Power Source

Refer to the [Connecting to Power Source](#) section of Chapter 2, [Installation and Configuration](#).

---

# Specifications

This appendix contains specifications for the NI PXIe-1062Q chassis.



**Caution** Specifications are subject to change without notice.

## Electrical

### AC Input

Input voltage range..... 100 to 240 VAC

Operating voltage range<sup>1</sup>..... 90 to 264 VAC

Input frequency ..... 50/60 Hz

Operating frequency range<sup>1</sup> ..... 47 to 63 Hz

Input current rating..... 8 A

Over-current protection..... 10 A circuit breaker

#### Line regulation

3.3 V.....  $<\pm 0.2\%$

5 V.....  $<\pm 0.1\%$

$\pm 12$  V .....  $<\pm 0.1\%$

Efficiency ..... 70% typical

---

<sup>1</sup> The operating range is guaranteed by design.

Power disconnect.....The AC power cable provides main power disconnect. The front-panel power switch causes the internal chassis power supply to provide DC power to the CompactPCI/PXI Express backplane. You also can use the rear-panel D-SUB 9-pin connector and power mode switch to control the internal chassis power supply.

## DC Output

DC current capacity ( $I_{MP}$ )

| Voltage            | Maximum Current |
|--------------------|-----------------|
| +3.3 V             | 32 A            |
| +5 V               | 30 A            |
| +12 V              | 25 A            |
| –12 V              | 1.5 A           |
| 5 V <sub>AUX</sub> | 2 A             |



**Note** Maximum total usable power is 353.6 W.

Backplane slot current capacity

| Slot                                         | +5 V | V (I/O) | +3.3 V | +12 V | –12 V | 5 V <sub>AUX</sub> |
|----------------------------------------------|------|---------|--------|-------|-------|--------------------|
| System Controller Slot                       | 15 A | —       | 15 A   | 30 A  | —     | 1 A                |
| System Timing Slot                           | —    | —       | 6 A    | 4 A   | —     | 1 A                |
| Hybrid Peripheral Slot with PXI-1 Peripheral | 6 A  | 5 A     | 6 A    | 1 A   | 1 A   | —                  |
| Hybrid Peripheral Slot with PXI-5 Peripheral | —    | —       | 6 A    | 4 A   | —     | 1 A                |
| PXI-1 Peripheral Slot                        | 6 A  | 11 A    | 6 A    | 1 A   | 1 A   | —                  |



**Notes** Total system slot current should not exceed 45 A.

PCI V(I/O) pins in PXI-1 peripheral slots and hybrid peripheral slots are connected to +5 V.

The maximum power dissipated in the system slot should not exceed 140 W.

The maximum power dissipated in a peripheral slot should not exceed 38.25 W.

#### Load regulation

| Voltage | Load Regulation |
|---------|-----------------|
| +3.3 V  | <5%             |
| +12 V   | <5%             |
| +5 V    | <5%             |
| –12 V   | <5%             |

#### Maximum ripple and noise (20 MHz bandwidth)

| Voltage | Maximum Ripple and Noise |
|---------|--------------------------|
| +3.3 V  | 50 mV <sub>pp</sub>      |
| +12 V   | 50 mV <sub>pp</sub>      |
| +5 V    | 50 mV <sub>pp</sub>      |
| –12 V   | 50 mV <sub>pp</sub>      |

Over-current protection..... All outputs protected from short circuit and overload with automatic recovery

#### Over-voltage protection

3.3 V and 5 V ..... Clamped at 20 to 30% above nominal output voltage

Power supply shuttle MTTR..... Replacement in under 5 minutes

# Chassis Cooling

|                                    |                                                                                                         |
|------------------------------------|---------------------------------------------------------------------------------------------------------|
| Module cooling system              |                                                                                                         |
| NI PXIe-1062Q .....                | Forced air circulation (positive pressurization) through two 110 cfm fans with High/Auto speed selector |
| Slot airflow direction .....       | Bottom of module to top of module                                                                       |
| Module cooling intake .....        | Bottom rear of chassis                                                                                  |
| Module cooling exhaust.....        | Along both sides and top of chassis                                                                     |
| Power supply cooling system .....  | Forced air circulation through integrated fan                                                           |
| Power supply cooling intake.....   | Right side of chassis                                                                                   |
| Power supply cooling exhaust ..... | Left side of chassis                                                                                    |

# Environmental

|                        |                                          |
|------------------------|------------------------------------------|
| Maximum altitude.....  | 2,000 m (800 mbar)<br>(at 25 °C ambient) |
| Pollution Degree ..... | 2                                        |
| For indoor use only.   |                                          |

# Operating Environment

|                                 |                                                                                                                                                                                  |
|---------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Ambient temperature range ..... | 0 to 55 °C<br>(Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.) |
| Relative humidity range.....    | 10 to 90%, noncondensing<br>(Tested in accordance with IEC-60068-2-56.)                                                                                                          |

## Storage Environment

|                                |                                                                                                                            |
|--------------------------------|----------------------------------------------------------------------------------------------------------------------------|
| Ambient temperature range..... | –40 to 71 °C<br>(Tested in accordance with<br>IEC-60068-2-1 and<br>IEC-60068-2-2. Meets<br>MIL-PRF-28800F Class 3 limits.) |
| Relative humidity range .....  | 5 to 95%, noncondensing<br>(Tested in accordance with<br>IEC-60068-2-56.)                                                  |

## Shock and Vibration

|                         |                                                                                                                                                                             |
|-------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Operational shock ..... | 30 g peak, half-sine, 11 ms pulse<br>(Tested in accordance with<br>IEC-60068-2-27. Meets<br>MIL-PRF-28800F Class 2 limits.)                                                 |
| Random Vibration        |                                                                                                                                                                             |
| Operating.....          | 5 to 500 Hz, 0.3 g <sub>rms</sub>                                                                                                                                           |
| Nonoperating.....       | 5 to 500 Hz, 2.4 g <sub>rms</sub><br>(Tested in accordance with<br>IEC-60068-2-64. Nonoperating<br>test profile exceeds the<br>requirements of<br>MIL-PRF-28800F, Class 3.) |

## Acoustic Emissions

### Sound Pressure Level (at Operator Position)

(Tested in accordance with ISO 7779. Meets MIL-PRF-28800F requirements.)

|                                       |          |
|---------------------------------------|----------|
| Auto fan (up to ~30 °C ambient) ..... | 43.6 dBA |
| High fan.....                         | 62 dBA   |

### Sound Power

|                                       |          |
|---------------------------------------|----------|
| Auto fan (up to ~30 °C ambient) ..... | 52.8 dBA |
| High fan.....                         | 72 dBA   |

## Safety

This product is designed to meet the requirements of the following standards of safety for information technology equipment:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1



**Note** For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

## Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326 (IEC 61326): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions



**Note** For the standards applied to assess the EMC of this product, refer to the *Online Product Certification* section.



**Note** For EMC compliance, operate this device with shielded cabling.

## CE Compliance

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

## Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit [ni.com/certification](http://ni.com/certification), search by model number or product line, and click the appropriate link in the Certification column.



## Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at [ni.com/environment](http://ni.com/environment). This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

## Waste Electrical and Electronic Equipment (WEEE)



**EU Customers** At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit [ni.com/environment/weee](http://ni.com/environment/weee).

## 电子信息产品污染控制管理办法（中国 RoHS）



**中国客户** National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 [ni.com/environment/rohs\\_china](http://ni.com/environment/rohs_china)。(For information about China RoHS compliance, go to [ni.com/environment/rohs\\_china](http://ni.com/environment/rohs_china).)

## Backplane

|                                     |                                                                                                                                                                                                                                                                 |
|-------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Size .....                          | 3U-sized; one system slot (with three system expansion slots) and seven peripheral slots.<br>Compliant with IEEE 1101.10 mechanical packaging.<br>PXI Express Specification compliant.<br>Accepts both PXI Express and CompactPCI (PICMG 2.0 R 3.0) 3U modules. |
| Backplane bare-board material ..... | UL 94 V-0 Recognized                                                                                                                                                                                                                                            |
| Backplane connectors .....          | Conforms to IEC 917 and IEC 1076-4-101, and are UL 94 V-0 rated                                                                                                                                                                                                 |

# System Synchronization Clocks

## (PXI\_CLK10, PXIe\_CLK100, PXIe\_SYNC100)

### 10 MHz System Reference Clock: PXI\_CLK10

|                                 |                                                                |
|---------------------------------|----------------------------------------------------------------|
| Maximum slot-to-slot skew ..... | 250 ps                                                         |
| Accuracy .....                  | ±25 ppm max. (guaranteed over the operating temperature range) |
| Maximum jitter .....            | 5 ps RMS phase-jitter<br>(10 Hz–1 MHz range)                   |
| Duty-factor.....                | 45%–55%                                                        |
| Unloaded signal swing.....      | 3.3 V ±0.3 V                                                   |



**Note** For other specifications refer to the *PXI-1 Hardware Specification*.

### 100 MHz System Reference Clock: PXIe\_CLK100 and PXIe-SYNC100

|                                                                                                              |                                                                                                 |
|--------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------|
| Maximum slot-to-slot skew .....                                                                              | 100 ps                                                                                          |
| Accuracy .....                                                                                               | ±25 ppm max. (guaranteed over the operating temperature range)                                  |
| Maximum jitter .....                                                                                         | 3 ps RMS phase-jitter<br>(10 Hz–12 kHz range)<br>2 ps RMS phase-jitter<br>(12 kHz–20 MHz range) |
| Duty-factor for PXIe_CLK100.....                                                                             | 45%–55%                                                                                         |
| Absolute differential voltage<br>(When terminated with a 50 Ω load<br>to 1.30 V or Thévenin equivalent)..... | 400–1000 mV                                                                                     |
| Single-ended V <sub>OH</sub> .....                                                                           | 2.0–2.5 V                                                                                       |



**Note** For other specifications, refer to the *PXI-5 PXI Express Hardware Specification*.

## External 10 MHz Reference Out (BNC on rear panel of chassis)

|                        |                                                                                            |
|------------------------|--------------------------------------------------------------------------------------------|
| Accuracy .....         | $\pm 25$ ppm max. (guaranteed over the operating temperature range)                        |
| Maximum jitter .....   | 5 ps RMS phase-jitter<br>(10 Hz–1 MHz range)                                               |
| Output amplitude.....  | 1 V <sub>pp</sub> $\pm 20\%$ square-wave<br>into 50 $\Omega$<br>2 V <sub>pp</sub> unloaded |
| Output impedance ..... | 50 $\Omega \pm 5 \Omega$                                                                   |

## External Clock Source

|                                                 |                                                                       |
|-------------------------------------------------|-----------------------------------------------------------------------|
| Frequency .....                                 | 10 MHz $\pm 100$ PPM                                                  |
| Input amplitude                                 |                                                                       |
| Rear panel BNC .....                            | 200 mV <sub>pp</sub> to 5 V <sub>pp</sub> square-wave<br>or sine-wave |
| System timing slot                              |                                                                       |
| PXI_CLK10_IN.....                               | 5 V or 3.3 V TTL signal                                               |
| Rear panel BNC input impedance.....             | 50 $\Omega \pm 5 \Omega$                                              |
| Maximum jitter introduced<br>by backplane ..... | 1 ps RMS phase-jitter<br>(10 Hz–1 MHz range)                          |

## PXIe\_SYNC\_CTRL

|                       |           |
|-----------------------|-----------|
| V <sub>IH</sub> ..... | 3.0–5.5 V |
| V <sub>IL</sub> ..... | 0–0.8 V   |

## PXI Star Trigger

|                                          |                      |
|------------------------------------------|----------------------|
| Maximum slot-to-slot skew .....          | 250 ps               |
| Backplane characteristic impedance ..... | 65 $\Omega \pm 10\%$ |



**Notes** For PXI slot to PXI Star mapping refer to the *System Timing Slot* section of Chapter 1, *Getting Started*.

For other specifications refer to the *PXI-1 Hardware Specification*.

## PXI Differential Star Triggers (PXIe-DSTARA, PXIe-DSTARB, PXIe-DSTARC)

Maximum slot-to-slot skew .....150 ps

Maximum differential skew .....25 ps

Backplane differential impedance .....100  $\Omega \pm 10\%$



**Notes** For PXIe slot to PXI\_DSTAR mapping refer to the *System Timing Slot* section of Chapter 1, *Getting Started*.

For other specifications, the NI PXIe-1062Q complies with the *PXI-5 PXI Express Hardware Specification*.

## DMA Support

For more information about this chassis' support of hardware modules with 64-bit DMA and/or 32-bit DMA with PAE mode, please visit [ni.com/info](http://ni.com/info) and enter the Info Code PXI64HANG.

## Mechanical

### Overall dimensions

#### Standard chassis

Height .....6.97 in. (177.1 mm)

Width .....10.68 in. (271.4 mm)

Depth .....15.61 in. (396.5 mm)



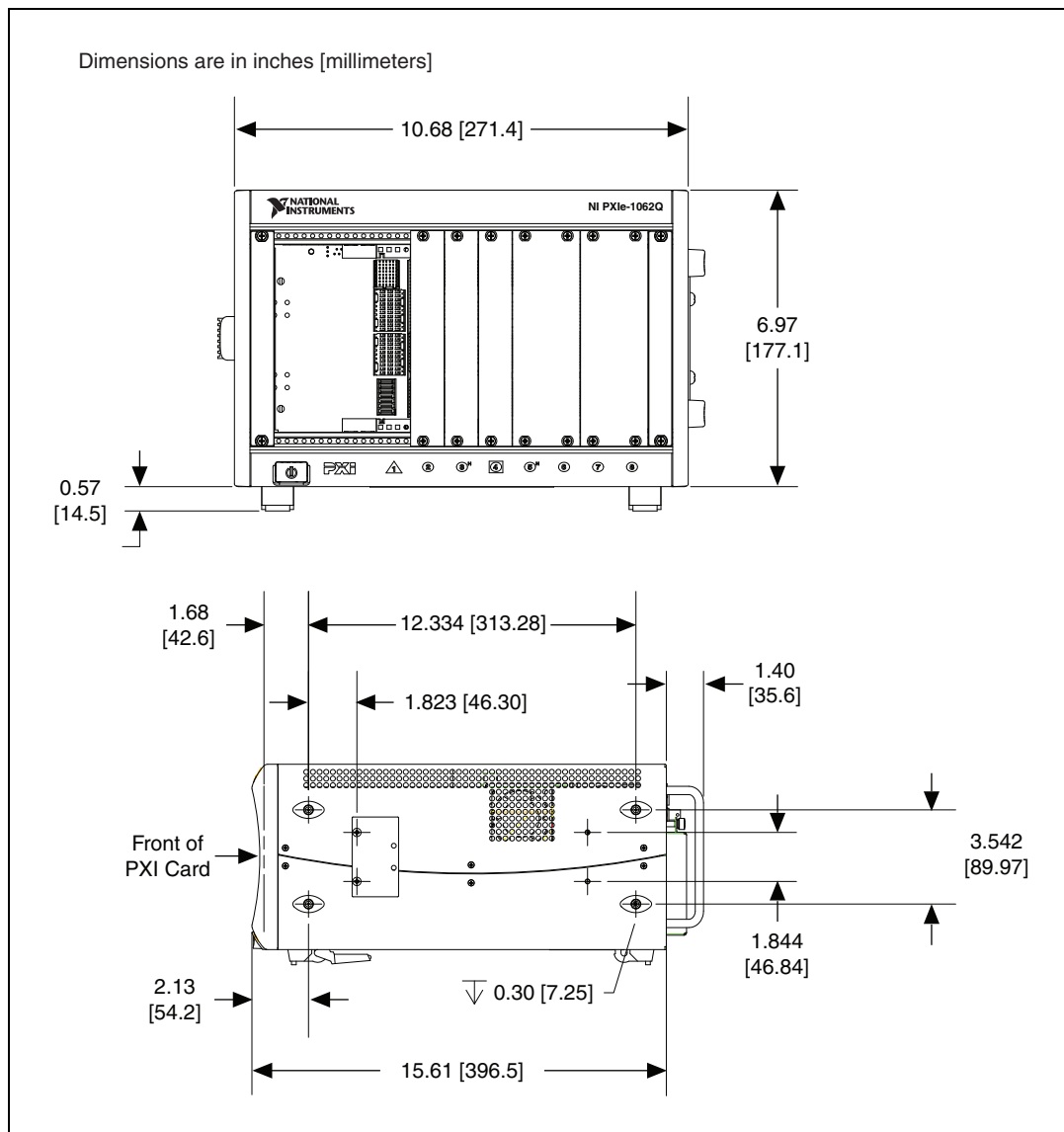
**Note** 0.57 in. (14.5 mm) is added to height when feet are installed. When tilted with front feet extended on table top, height is increased approximately 2.08 in. (52.8 mm) in front and 0.583 in. (14.8 mm) in rear.

Weight .....8.8 kg (19.4 lb)

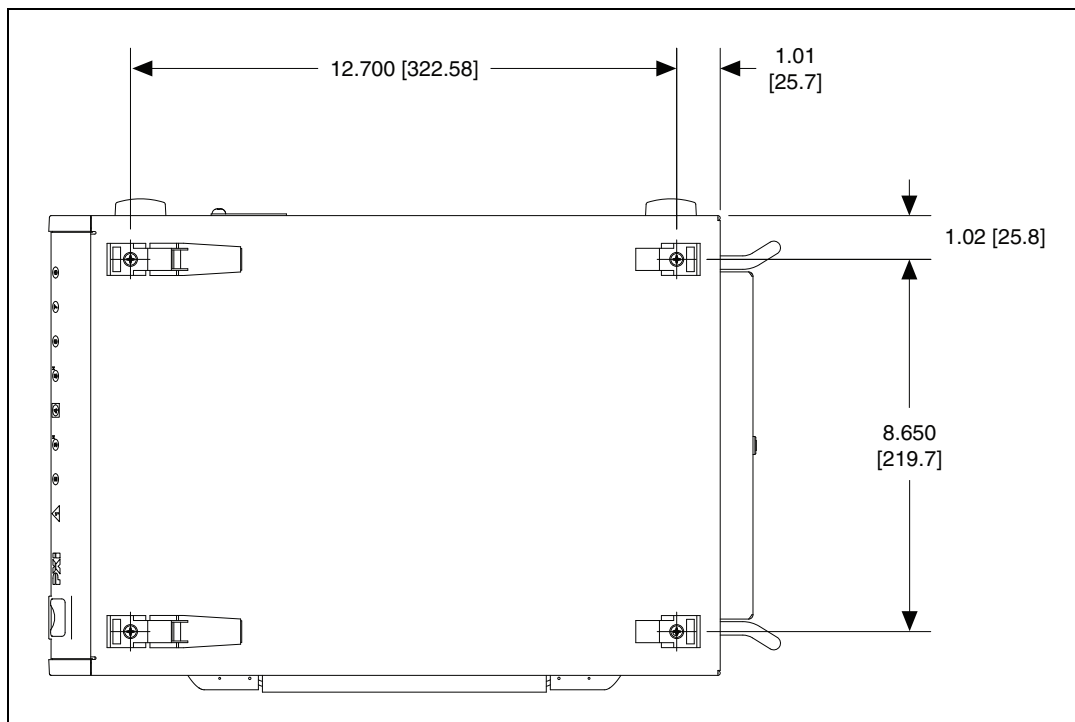
Chassis materials .....Sheet Aluminum (5052-H32,  
3003-H14, and 6061-T6),  
Extruded Aluminum (6060-T6),  
and Cold Rolled Steel, PC-ABS,  
Santoprene, Nylon

Finish..... Conductive Clear Iridite  
on Aluminum  
Clear Chromate Zinc Plating  
on Cold Rolled Steel  
Polyurethane Enamel

Figures A-1 and A-2 show the NI PXIe-1062Q chassis dimensions. The holes shown are for the installation of the optional rack mount kits. You can install those kits on the front or rear of the chassis, depending on which end of the chassis you want to face toward the front of the instrument cabinet. Notice that the front and rear chassis mounting holes (size M4) are symmetrical.

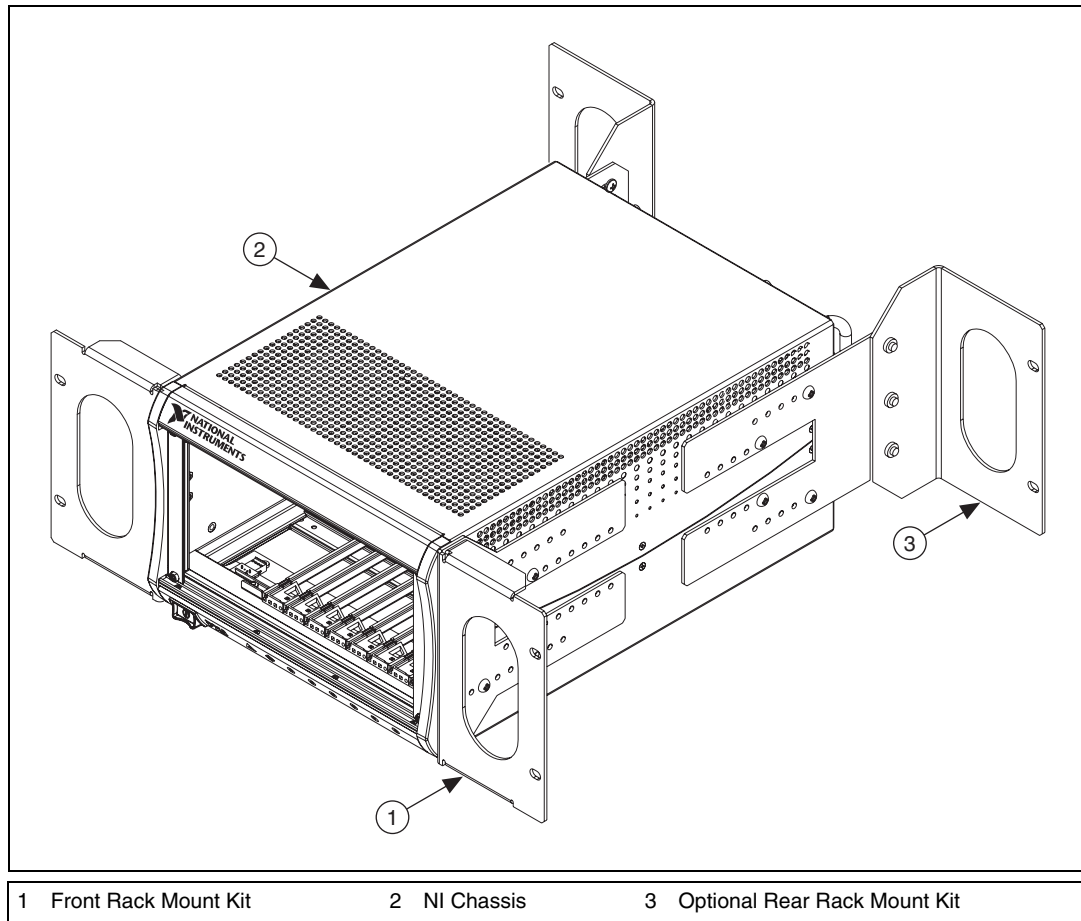


**Figure A-1.** NI PXIe-1062Q Chassis Dimensions (Front and Side)



**Figure A-2.** NI PXIe-1062Q Chassis Dimensions (Bottom)

Figure A-3 shows the chassis rack mount kit components.



**Figure A-3.** NI Chassis Rack Mount Kit Components



**Note** The chassis shown in Figure A-3 is representative of the NI PXI-1042/NI PXIe-1062Q product line.



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# Pinouts

This appendix describes the connector pinouts for the NI PXIe-1062Q chassis backplane.

Table B-1 shows the XP1 Connector Pinout for the System Controller slot.

Table B-2 shows the XP2 Connector Pinout for the System Controller slot.

Table B-3 shows the XP3 Connector Pinout for the System Controller slot.

Table B-4 shows the XP4 Connector Pinout for the System Controller slot.

Table B-5 shows the TP2 Connector Pinout for the System Timing slot.

Table B-6 shows the XP3 Connector Pinout for the System Timing slot.

Table B-7 shows the XP4 Connector Pinout for the System Timing slot.

Table B-8 shows the P1 Connector Pinout for the Peripheral slots.

Table B-9 shows the P2 Connector Pinout for the Peripheral slots.

Table B-10 shows the P1 Connector Pinout for the Hybrid Peripheral slots.

Table B-11 shows the XP3 Connector Pinout for the Hybrid Peripheral slots.

Table B-12 shows the XP4 Connector Pinout for the Hybrid Peripheral slots.

For more detailed information, refer to the *PXI-5 PXI Express Hardware Specification*, Revision 2.0. Contact the PXI Systems Alliance for a copy of the specification.

# System Controller Slot Pinouts

**Table B-1.** XP1 Connector Pinout for the System Controller Slot

| Pins | Signals |
|------|---------|
| A    | GND     |
| B    | 12V     |
| C    | 12V     |
| D    | GND     |
| E    | 5V      |
| F    | 3.3V    |
| G    | GND     |

**Table B-2.** XP2 Connector Pinout for the System Controller Slot

| Pin | A      | B      | ab  | C      | D      | cd  | E      | F      | ef  |
|-----|--------|--------|-----|--------|--------|-----|--------|--------|-----|
| 1   | 3PETp1 | 3PETn1 | GND | 3PERp1 | 3PERn1 | GND | 3PETp2 | 3PETn2 | GND |
| 2   | 3PETp3 | 3PETn3 | GND | 3PERp3 | 3PERn3 | GND | 3PERp2 | 3PERn2 | GND |
| 3   | 4PETp0 | 4PETn0 | GND | 4PERp0 | 4PERn0 | GND | 4PETp1 | 4PETn1 | GND |
| 4   | 4PETp2 | 4PETn2 | GND | 4PERp2 | 4PERn2 | GND | 4PERp1 | 4PERn1 | GND |
| 5   | 4PETp3 | 4PETn3 | GND | 4PERp3 | 4PERn3 | GND | RSV    | RSV    | GND |
| 6   | RSV    | RSV    | GND | RSV    | RSV    | GND | RSV    | RSV    | GND |
| 7   | RSV    | RSV    | GND | RSV    | RSV    | GND | RSV    | RSV    | GND |
| 8   | RSV    | RSV    | GND | RSV    | RSV    | GND | RSV    | RSV    | GND |
| 9   | RSV    | RSV    | GND | RSV    | RSV    | GND | RSV    | RSV    | GND |
| 10  | RSV    | RSV    | GND | RSV    | RSV    | GND | RSV    | RSV    | GND |

**Table B-3.** XP3 Connector Pinout for the System Controller Slot

| Pin | A      | B      | ab  | C        | D        | cd  | E        | F        | ef  |
|-----|--------|--------|-----|----------|----------|-----|----------|----------|-----|
| 1   | RSV    | RSV    | GND | RSV      | RSV      | GND | RSV      | RSV      | GND |
| 2   | RSV    | RSV    | GND | PWR_OK   | PS_ON#   | GND | LINKCAP  | PWRBTN#  | GND |
| 3   | SMBDAT | SMBCLK | GND | 4RefClk+ | 4RefClk– | GND | 2RefClk+ | 2RefClk– | GND |
| 4   | RSV    | PERST# | GND | 3RefClk+ | 3RefClk– | GND | 1RefClk+ | 1RefClk– | GND |
| 5   | 1PETp0 | 1PETn0 | GND | 1PERp0   | 1PERn0   | GND | 1PETp1   | 1PETn1   | GND |
| 6   | 1PETp2 | 1PETn2 | GND | 1PERp2   | 1PERn2   | GND | 1PERp1   | 1PERn1   | GND |
| 7   | 1PETp3 | 1PETn3 | GND | 1PERp3   | 1PERn3   | GND | 2PETp0   | 2PETn0   | GND |
| 8   | 2PETp1 | 2PETn1 | GND | 2PERp1   | 2PERn1   | GND | 2PERp0   | 2PERn0   | GND |
| 9   | 2PETp2 | 2PETn2 | GND | 2PERp2   | 2PERn2   | GND | 2PETp3   | 2PETn3   | GND |
| 10  | 3PETp0 | 3PETn0 | GND | 3PERp0   | 3PERn0   | GND | 2PERp3   | 2PERn3   | GND |

**Table B-4.** XP4 Connector Pinout for the System Controller Slot

| Pin | Z   | A         | B         | C         | D        | E         | F   |
|-----|-----|-----------|-----------|-----------|----------|-----------|-----|
| 1   | GND | GA4       | GA3       | GA2       | GA1      | GA0       | GND |
| 2   | GND | 5Vaux     | GND       | SYSEN#    | WAKE#    | ALERT#    | GND |
| 3   | GND | RSV       | RSV       | RSV       | RSV      | RSV       | GND |
| 4   | GND | RSV       | RSV       | RSV       | RSV      | RSV       | GND |
| 5   | GND | PXI_TRIG3 | PXI_TRIG4 | PXI_TRIG5 | GND      | PXI_TRIG6 | GND |
| 6   | GND | PXI_TRIG2 | GND       | RSV       | PXI_STAR | PXI_CLK10 | GND |
| 7   | GND | PXI_TRIG1 | PXI_TRIG0 | RSV       | GND      | PXI_TRIG7 | GND |
| 8   | GND | RSV       | GND       | RSV       | RSV      | PXI_LBR6  | GND |

# System Timing Slot Pinouts

**Table B-5.** TP2 Connector Pinout for the System Timing Slot

| Pin | A             | B             | ab  | C             | D             | cd  | E             | F             | ef  |
|-----|---------------|---------------|-----|---------------|---------------|-----|---------------|---------------|-----|
| 1   | PXIe_DSTARC0+ | PXIe_DSTARC0– | GND | PXIe_DSTARC8+ | PXIe_DSTARC8– | GND | PXIe_DSTARB8+ | PXIe_DSTARB8– | GND |
| 2   | PXIe_DSTARA0+ | PXIe_DSTARA0– | GND | PXIe_DSTARC9+ | PXIe_DSTARC9– | GND | PXIe_DSTARA8+ | PXIe_DSTARA8– | GND |
| 3   | PXIe_DSTARB0+ | PXIe_DSTARB0– | GND | NC            | NC            | GND | PXIe_DSTARA9+ | PXIe_DSTARA9– | GND |
| 4   | NC            | NC            | GND | PXI_STAR0     | PXI_STAR1     | GND | PXIe_DSTARB9+ | PXIe_DSTARB9– | GND |
| 5   | NC            | NC            | GND | PXI_STAR2     | PXI_STAR3     | GND | NC            | NC            | GND |
| 6   | NC            | NC            | GND | PXI_STAR4     | PXI_STAR5     | GND | NC            | NC            | GND |
| 7   | NC            | NC            | GND | PXI_STAR6     | NC            | GND | NC            | NC            | GND |
| 8   | NC            | NC            | GND | NC            | NC            | GND | NC            | NC            | GND |
| 9   | NC            | NC            | GND | NC            | NC            | GND | NC            | NC            | GND |
| 10  | NC            | NC            | GND | NC            | NC            | GND | NC            | NC            | GND |

**Table B-6.** XP3 Connector Pinout for the System Timing Slot

| Pin | A            | B            | ab  | C             | D             | cd  | E            | F            | ef  |
|-----|--------------|--------------|-----|---------------|---------------|-----|--------------|--------------|-----|
| 1   | PXIe_CLK100+ | PXIe_CLK100– | GND | PXIe_SYNC100+ | PXIe_SYNC100– | GND | PXIe_DSTARC+ | PXIe_DSTARC– | GND |
| 2   | PRSENT#      | PWREN#       | GND | PXIe_DSTARB+  | PXIe_DSTARB–  | GND | PXIe_DSTARA+ | PXIe_DSTARA– | GND |
| 3   | SMBDAT       | SMBCLK       | GND | RSV           | RSV           | GND | RSV          | RSV          | GND |
| 4   | MPWRGD*      | PERST#       | GND | RSV           | RSV           | GND | lRefClk+     | lRefClk–     | GND |
| 5   | lPETp0       | lPETn0       | GND | lPERp0        | lPERn0        | GND | lPETp1       | lPETn1       | GND |
| 6   | lPETp2       | lPETn2       | GND | lPERp2        | lPERn2        | GND | lPERp1       | lPERn1       | GND |
| 7   | lPETp3       | lPETn3       | GND | lPERp3        | lPERn3        | GND | lPETp4       | lPETn4       | GND |
| 8   | lPETp5       | lPETn5       | GND | lPERp5        | lPERn5        | GND | lPERp4       | lPERn4       | GND |
| 9   | lPETp6       | lPETn6       | GND | lPERp6        | lPERn6        | GND | lPETp7       | lPETn7       | GND |
| 10  | RSV          | RSV          | GND | RSV           | RSV           | GND | lPERp7       | lPERn7       | GND |

**Table B-7.** XP4 Connector Pinout for the System Timing Slot

| Pin | Z   | A              | B         | C         | D            | E         | F   |
|-----|-----|----------------|-----------|-----------|--------------|-----------|-----|
| 1   | GND | GA4            | GA3       | GA2       | GA1          | GA0       | GND |
| 2   | GND | 5Vaux          | GND       | SYSEN#    | WAKE#        | ALERT#    | GND |
| 3   | GND | 12V            | 12V       | GND       | GND          | GND       | GND |
| 4   | GND | GND            | GND       | 3.3V      | 3.3V         | 3.3V      | GND |
| 5   | GND | PXI_TRIG3      | PXI_TRIG4 | PXI_TRIG5 | GND          | PXI_TRIG6 | GND |
| 6   | GND | PXI_TRIG2      | GND       | ATNLED    | PXI_CLK10_IN | PXI_CLK10 | GND |
| 7   | GND | PXI_TRIG1      | PXI_TRIG0 | ATNSW#    | GND          | PXI_TRIG7 | GND |
| 8   | GND | PXIe_SYNC_CTRL | GND       | RSV       | PXI_LBL6     | PXI_LBR6  | GND |

# Peripheral Slot Pinouts

**Table B-8.** P1 Connector Pinout for the Peripheral Slot

| Pin   | Z        | A        | B        | C        | D       | E        | F   |
|-------|----------|----------|----------|----------|---------|----------|-----|
| 25    | GND      | 5V       | REQ64#   | ENUM#    | 3.3V    | 5V       | GND |
| 24    | GND      | AD[1]    | 5V       | V(I/O)   | AD[0]   | ACK64#   | GND |
| 23    | GND      | 3.3V     | AD[4]    | AD[3]    | 5V      | AD[2]    | GND |
| 22    | GND      | AD[7]    | GND      | 3.3V     | AD[6]   | AD[5]    | GND |
| 21    | GND      | 3.3V     | AD[9]    | AD[8]    | M66EN   | C/BE[0]# | GND |
| 20    | GND      | AD[12]   | GND      | V(I/O)   | AD[11]  | AD[10]   | GND |
| 19    | GND      | 3.3V     | AD[15]   | AD[14]   | GND     | AD[13]   | GND |
| 18    | GND      | SERR#    | GND      | 3.3V     | PAR     | C/BE[1]# | GND |
| 17    | GND      | 3.3V     | IPMB_SCL | IPMB_SDA | GND     | PERR#    | GND |
| 16    | GND      | DEVSEL#  | GND      | V(I/O)   | STOP#   | LOCK#    | GND |
| 15    | GND      | 3.3V     | FRAME#   | IRDY#    | BD_SEL# | TRDY#    | GND |
| 12–14 | Key Area |          |          |          |         |          |     |
| 11    | GND      | AD[18]   | AD[17]   | AD[16]   | GND     | C/BE[2]# | GND |
| 10    | GND      | AD[21]   | GND      | 3.3V     | AD[20]  | AD[19]   | GND |
| 9     | GND      | C/BE[3]# | IDSEL    | AD[23]   | GND     | AD[22]   | GND |
| 8     | GND      | AD[26]   | GND      | V(I/O)   | AD[25]  | AD[24]   | GND |
| 7     | GND      | AD[30]   | AD[29]   | AD[28]   | GND     | AD[27]   | GND |
| 6     | GND      | REQ#     | GND      | 3.3V     | CLK     | AD[31]   | GND |
| 5     | GND      | BRSVP1A5 | BRSVP1B5 | RST#     | GND     | GNT#     | GND |
| 4     | GND      | IPMB_PWR | HEALTHY  | V(I/O)   | INTP    | INTS     | GND |
| 3     | GND      | INTA#    | INTB#    | INTC#    | 5V      | INTD#    | GND |
| 2     | GND      | TCK      | 5V       | TMS      | TDO     | TDI      | GND |
| 1     | GND      | 5V       | –12V     | TRST#    | +12V    | 5V       | GND |

**Table B-9.** P2 Connector Pinout for the Peripheral Slot

| Pin | Z   | A           | B         | C         | D         | E         | F   |
|-----|-----|-------------|-----------|-----------|-----------|-----------|-----|
| 22  | GND | GA4         | GA3       | GA2       | GA1       | GA0       | GND |
| 21  | GND | PXI_LBR0    | GND       | PXI_LBR1  | PXI_LBR2  | PXI_LBR3  | GND |
| 20  | GND | PXI_LBR4    | PXI_LBR5  | PXI_LBL0  | GND       | PXI_LBL1  | GND |
| 19  | GND | PXI_LBL2    | GND       | PXI_LBL3  | PXI_LBL4  | PXI_LBL5  | GND |
| 18  | GND | PXI_TRIG3   | PXI_TRIG4 | PXI_TRIG5 | GND       | PXI_TRIG6 | GND |
| 17  | GND | PXI_TRIG2   | GND       | RSV       | PXI_STAR  | PXI_CLK10 | GND |
| 16  | GND | PXI_TRIG1   | PXI_TRIG0 | RSV       | GND       | PXI_TRIG7 | GND |
| 15  | GND | PXI_BRSVA15 | GND       | RSV       | PXI_LBL6  | PXI_LBR6  | GND |
| 14  | GND | RSV         | RSV       | RSV       | GND       | RSV       | GND |
| 13  | GND | RSV         | GND       | V(I/O)    | RSV       | RSV       | GND |
| 12  | GND | RSV         | RSV       | RSV       | GND       | RSV       | GND |
| 11  | GND | RSV         | GND       | V(I/O)    | RSV       | RSV       | GND |
| 10  | GND | RSV         | RSV       | RSV       | GND       | RSV       | GND |
| 9   | GND | RSV         | GND       | V(I/O)    | RSV       | RSV       | GND |
| 8   | GND | RSV         | RSV       | RSV       | GND       | RSV       | GND |
| 7   | GND | RSV         | GND       | V(I/O)    | RSV       | RSV       | GND |
| 6   | GND | RSV         | RSV       | RSV       | GND       | RSV       | GND |
| 5   | GND | RSV         | GND       | V(I/O)    | RSV       | RSV       | GND |
| 4   | GND | V(I/O)      | 64EN#     | RSV       | GND       | RSV       | GND |
| 3   | GND | PXI_LBR7    | GND       | PXI_LBR8  | PXI_LBR9  | PXI_LBR10 | GND |
| 2   | GND | PXI_LBR11   | PXI_LBR12 | UNC       | PXI_LBL7  | PXI_LBL8  | GND |
| 1   | GND | PXI_LBL9    | GND       | PXI_LBL10 | PXI_LBL11 | PXI_LBL12 | GND |

# Hybrid Slot Pinouts

**Table B-10.** P1 Connector Pinout for the Hybrid Slot

| Pin   | Z        | A        | B        | C        | D       | E        | F   |
|-------|----------|----------|----------|----------|---------|----------|-----|
| 25    | GND      | 5V       | REQ64#   | ENUM#    | 3.3V    | 5V       | GND |
| 24    | GND      | AD[1]    | 5V       | V(I/O)   | AD[0]   | ACK64#   | GND |
| 23    | GND      | 3.3V     | AD[4]    | AD[3]    | 5V      | AD[2]    | GND |
| 22    | GND      | AD[7]    | GND      | 3.3V     | AD[6]   | AD[5]    | GND |
| 21    | GND      | 3.3V     | AD[9]    | AD[8]    | M66EN   | C/BE[0]# | GND |
| 20    | GND      | AD[12]   | GND      | V(I/O)   | AD[11]  | AD[10]   | GND |
| 19    | GND      | 3.3V     | AD[15]   | AD[14]   | GND     | AD[13]   | GND |
| 18    | GND      | SERR#    | GND      | 3.3V     | PAR     | C/BE[1]# | GND |
| 17    | GND      | 3.3V     | IPMB_SCL | IPMB_SDA | GND     | PERR#    | GND |
| 16    | GND      | DEVSEL#  | GND      | V(I/O)   | STOP#   | LOCK#    | GND |
| 15    | GND      | 3.3V     | FRAME#   | IRDY#    | BD_SEL# | TRDY#    | GND |
| 12–14 | Key Area |          |          |          |         |          |     |
| 11    | GND      | AD[18]   | AD[17]   | AD[16]   | GND     | C/BE[2]# | GND |
| 10    | GND      | AD[21]   | GND      | 3.3V     | AD[20]  | AD[19]   | GND |
| 9     | GND      | C/BE[3]# | IDSEL    | AD[23]   | GND     | AD[22]   | GND |
| 8     | GND      | AD[26]   | GND      | V(I/O)   | AD[25]  | AD[24]   | GND |
| 7     | GND      | AD[30]   | AD[29]   | AD[28]   | GND     | AD[27]   | GND |
| 6     | GND      | REQ#     | GND      | 3.3V     | CLK     | AD[31]   | GND |
| 5     | GND      | BRSVP1A5 | BRSVP1B5 | RST#     | GND     | GNT#     | GND |
| 4     | GND      | IPMB_PWR | HEALTHY# | V(I/O)   | INTP    | INTS     | GND |
| 3     | GND      | INTA#    | INTB#    | INTC#    | 5V      | INTD#    | GND |
| 2     | GND      | TCK      | 5V       | TMS      | TDO     | TDI      | GND |
| 1     | GND      | 5V       | –12V     | TRST#    | +12V    | 5V       | GND |



**Table B-11.** XP3 Connector Pinout for the Hybrid Slot

| Pin | A            | B            | ab  | C             | D             | cd  | E            | F            | ef  |
|-----|--------------|--------------|-----|---------------|---------------|-----|--------------|--------------|-----|
| 1   | PXIe_CLK100+ | PXIe_CLK100– | GND | PXIe_SYNC100+ | PXIe_SYNC100– | GND | PXIe_DSTARC+ | PXIe_DSTARC– | GND |
| 2   | PRSNT#       | PWREN#       | GND | PXIe_DSTARB+  | PXIe_DSTARB–  | GND | PXIe_DSTARA+ | PXIe_DSTARA– | GND |
| 3   | SMBDAT       | SMBCLK       | GND | RSV           | RSV           | GND | RSV          | RSV          | GND |
| 4   | MPWRGD*      | PERST#       | GND | RSV           | RSV           | GND | 1RefClk+     | 1RefClk–     | GND |
| 5   | 1PETp0       | 1PETn0       | GND | 1PERp0        | 1PERn0        | GND | 1PETp1       | 1PETn1       | GND |
| 6   | 1PETp2       | 1PETn2       | GND | 1PERp2        | 1PERn2        | GND | 1PERp1       | 1PERn1       | GND |
| 7   | 1PETp3       | 1PETn3       | GND | 1PERp3        | 1PERn3        | GND | 1PETp4       | 1PETn4       | GND |
| 8   | 1PETp5       | 1PETn5       | GND | 1PERp5        | 1PERn5        | GND | 1PERp4       | 1PERn4       | GND |
| 9   | 1PETp6       | 1PETn6       | GND | 1PERp6        | 1PERn6        | GND | 1PETp7       | 1PETn7       | GND |
| 10  | RSV          | RSV          | GND | RSV           | RSV           | GND | 1PERp7       | 1PERn7       | GND |

**Table B-12.** XP4 Connector Pinout for the Hybrid Slot

| Pin | Z   | A         | B         | C         | D        | E         | F   |
|-----|-----|-----------|-----------|-----------|----------|-----------|-----|
| 1   | GND | GA4       | GA3       | GA2       | GA1      | GA0       | GND |
| 2   | GND | 5Vaux     | GND       | SYSEN#    | WAKE#    | ALERT#    | GND |
| 3   | GND | 12V       | 12V       | GND       | GND      | GND       | GND |
| 4   | GND | GND       | GND       | 3.3V      | 3.3V     | 3.3V      | GND |
| 5   | GND | PXI_TRIG3 | PXI_TRIG4 | PXI_TRIG5 | GND      | PXI_TRIG6 | GND |
| 6   | GND | PXI_TRIG2 | GND       | ATNLED    | PXI_STAR | PXI_CLK10 | GND |
| 7   | GND | PXI_TRIG1 | PXI_TRIG0 | ATNSW#    | GND      | PXI_TRIG7 | GND |
| 8   | GND | RSV       | GND       | RSV       | PXI_LBL6 | PXI_LBR6  | GND |



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# Glossary

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| Symbol | Prefix | Value      |
|--------|--------|------------|
| p      | pico   | $10^{-12}$ |
| n      | nano   | $10^{-9}$  |
| $\mu$  | micro  | $10^{-6}$  |
| m      | milli  | $10^{-3}$  |
| k      | kilo   | $10^3$     |
| M      | mega   | $10^6$     |
| G      | giga   | $10^9$     |
| T      | tera   | $10^{12}$  |

## Symbols

|        |                        |
|--------|------------------------|
| °      | Degrees.               |
| $\geq$ | Equal or greater than. |
| $\leq$ | Equal or less than.    |
| %      | Percent.               |

## A

|      |                                        |
|------|----------------------------------------|
| A    | Amperes.                               |
| AC   | Alternating current.                   |
| ANSI | American National Standards Institute. |
| Auto | Automatic fan speed control.           |
| AWG  | American Wire Gauge.                   |

## **B**

**backplane** An assembly, typically a printed circuit board, with connectors and signal paths that bus the connector pins.

**BNC** Bayonet Neill Concelman connector; a commonly used coaxial connector.

## **C**

**C** Celsius.

**cfm** Cubic feet per minute.

**CFR** Code of Federal Regulations.

**cm** Centimeters.

**CompactPCI** An adaptation of the Peripheral Component Interconnect (PCI) Specification 2.1 or later for industrial and/or embedded applications requiring a more robust mechanical form factor than desktop PCI. It uses industry standard mechanical components and high-performance connector technologies to provide an optimized system intended for rugged applications. It is electrically compatible with the PCI Specification, which enables low-cost PCI components to be utilized in a mechanical form factor suited for rugged environments.

**CSA** Canadian Standards Association.

## **D**

**daisy-chain** A method of propagating signals along a bus, in which the devices are prioritized on the basis of their position on the bus.

**DB-9** A 9-pin D-SUB connector.

**DC** Direct current.

**DoC** Declaration of Conformity.

**D-SUB** Subminiature D connector.

**E**

|            |                                                                  |
|------------|------------------------------------------------------------------|
| efficiency | Ratio of output power to input power, expressed as a percentage. |
| EIA        | Electronic Industries Association.                               |
| EMC        | Electromagnetic Compatibility.                                   |
| EMI        | Electromagnetic Interference.                                    |

**F**

|              |                                                                     |
|--------------|---------------------------------------------------------------------|
| FCC          | Federal Communications Commission.                                  |
| filler panel | A blank module front panel used to fill empty slots in the chassis. |

**G**

|                  |                                                                                                                |
|------------------|----------------------------------------------------------------------------------------------------------------|
| g                | (1) grams; (2) a measure of acceleration equal to $9.8 \text{ m/s}^2$ .                                        |
| GPIO             | General Purpose Interface Bus (IEEE 488).                                                                      |
| $g_{\text{RMS}}$ | A measure of random vibration. The root mean square of acceleration levels in a random vibration test profile. |

**H**

|    |                           |
|----|---------------------------|
| hr | Hours.                    |
| Hz | Hertz; cycles per second. |

**I**

|                 |                                                                                                                          |
|-----------------|--------------------------------------------------------------------------------------------------------------------------|
| IEC             | International Electrotechnical Commission; an organization that sets international electrical and electronics standards. |
| IEEE            | Institute of Electrical and Electronics Engineers.                                                                       |
| $I_{\text{MP}}$ | Mainframe peak current.                                                                                                  |

in. Inches.

inhibit To turn off.

## **J**

jitter A measure of the small, rapid variations in clock transition times from their nominal regular intervals. Units: seconds RMS.

## **K**

kg Kilograms.

km Kilometers.

## **L**

lb Pounds.

LED Light emitting diode.

line regulation The maximum steady-state percentage that a DC voltage output will change as a result of a specified change in input AC voltage (step change from 90 to 132 VAC or 180 to 264 VAC).

load regulation The maximum steady-state percentage that a DC voltage output will change as a result of a step change from no-load to full-load output current.

## **M**

m Meters.

MHz Megahertz. One million Hertz; one Hertz equals one cycle per second.

mi Miles.

ms Milliseconds.

MTBF Mean time between failure.

MTTR Mean time to repair.

**N**

NEMA National Electrical Manufacturers Association.

NI National Instruments.

**P**

power supply shuttle A removable module that contains the chassis power supply.

PXI PCI eXtensions for Instrumentation.

PXI\_CLK10 10 MHz PXI system reference clock.

**R**

RH Relative humidity.

RMS Root mean square.

**S**

s Seconds.

skew Deviation in signal transmission times.

slot blocker An assembly installed into an empty slot to improve the airflow in adjacent slots.

standby The backplane is unpowered (off), but the chassis is still connected to AC power mains.

System controller A module configured for installation in Slot 1 of a PXI chassis. This device is unique in the PXI system in that it performs the system controller functions, including clock sourcing and arbitration for data transfers across the backplane. Installing such a device into any other slot can damage the device, the PXI backplane, or both.



system reference clock

A 10 MHz clock, also called PXI\_CLK10, that is distributed to all peripheral slots in the chassis, as well as a BNC connector on the rear of chassis labeled *10 MHz REF OUT*. The system reference clock can be used for synchronization of multiple modules in a measurement or control system. The 10 MHz REF IN and OUT BNC connectors on the rear of the chassis can be used to synchronize multiple chassis to one reference clock. The PXI backplane specification defines implementation guidelines for PXI\_CLK10.

System Timing slot

This slot is located at slot 4 and has dedicated trigger lines to other slots.

## T

TTL

Transistor-transistor logic.

## U

UL

Underwriter's Laboratories.

## V

V

Volts.

VAC

Volts alternating current.

$V_{pp}$

Peak-to-peak voltage.

## W

W

Watts.

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